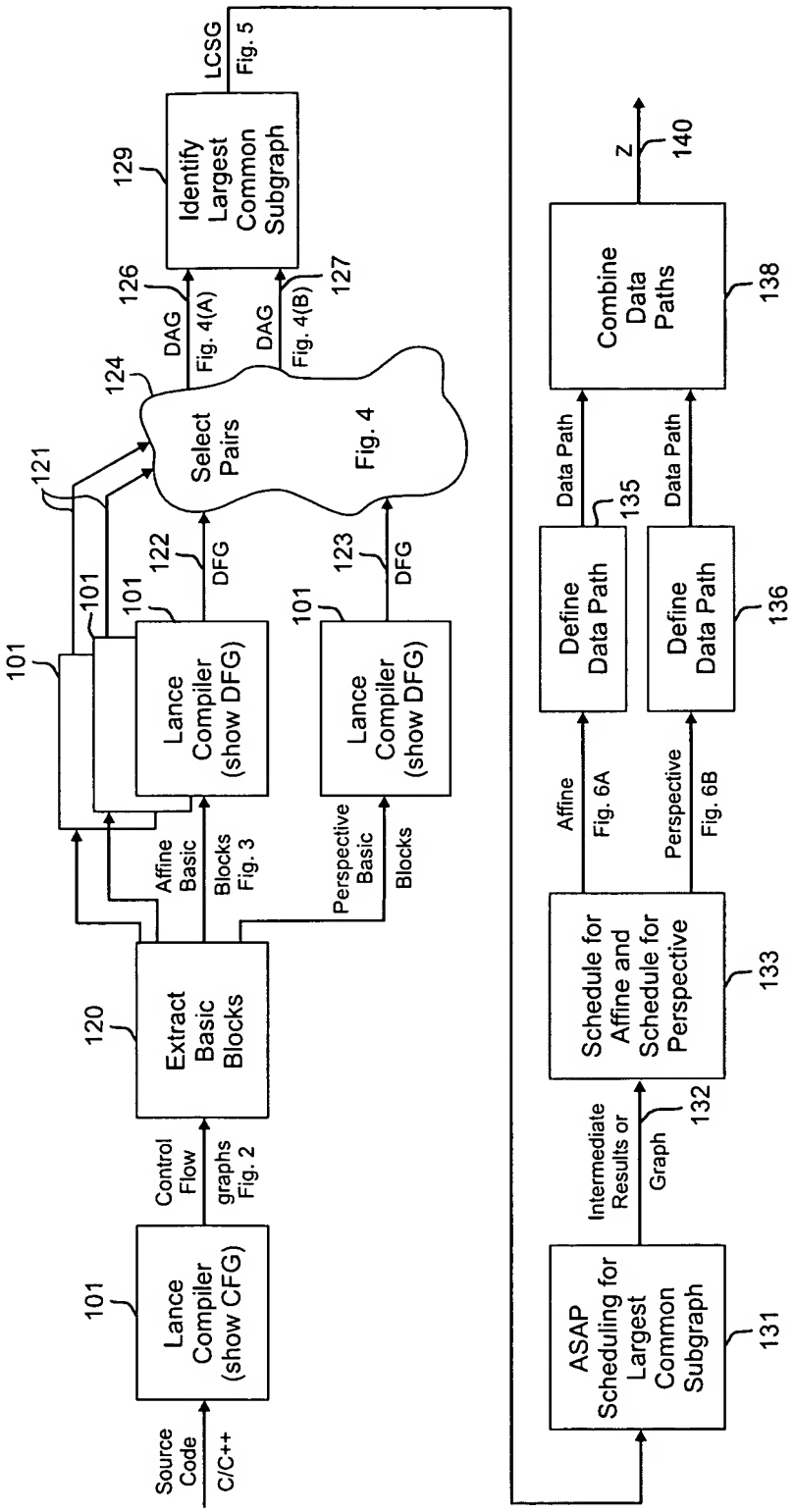

Source Code
C/C++
Lance Compiler (show CFG)
101
Control Flow graphs Fig. 2
Extract Basic Blocks
120
Affine Basic Blocks Fig. 3
Perspective Basic Blocks
Lance Compiler (show DFG)
Lance Compiler (show DFG)
101
101
101
101
121
122
123
DFG
DFG
Select Pairs
Fig. 4
124
DAG Fig. 4(A)
DAG Fig. 4(B)
126
127
Identify Largest Common Subgraph
129
LCSG Fig. 5
ASAP Scheduling for Largest Common Subgraph
131
Intermediate Results or Graph
132
Schedule for Affine and Schedule for Perspective
133
Affine Fig. 6A
Perspective Fig. 6B
Define Data Path
Define Data Path
135
136
Data Path
Data Path
Combine Data Paths
138
Z
140

Fig. 1

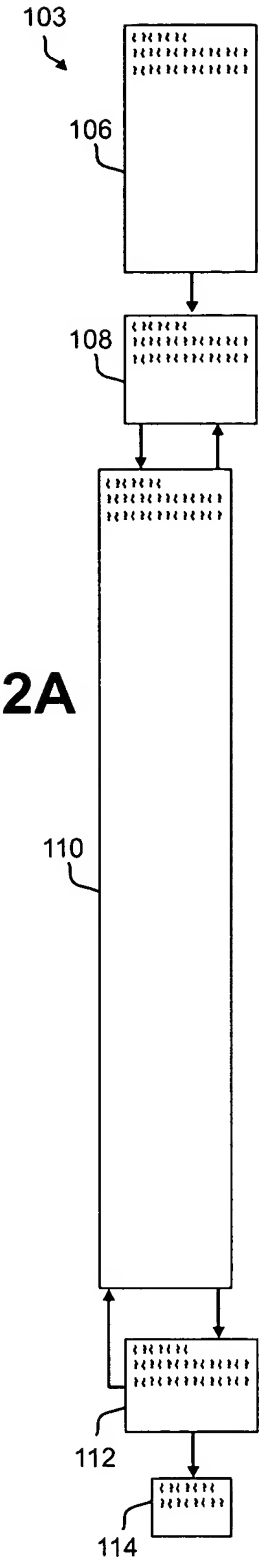


Fig. 2A

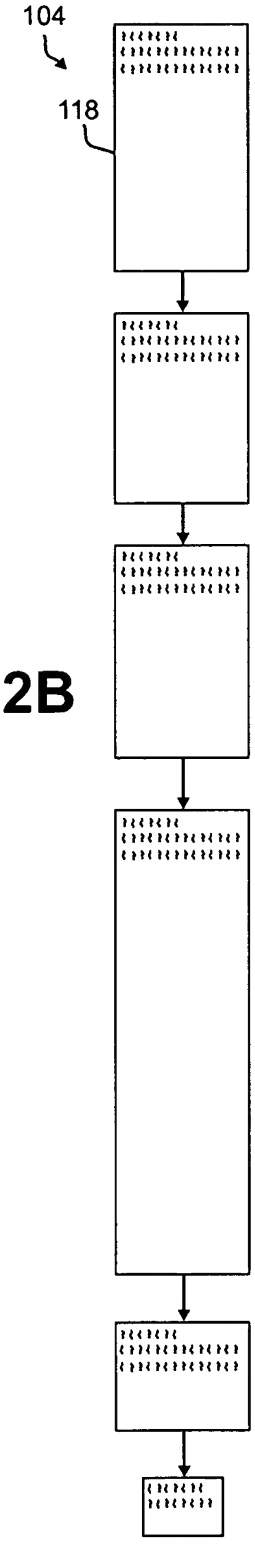
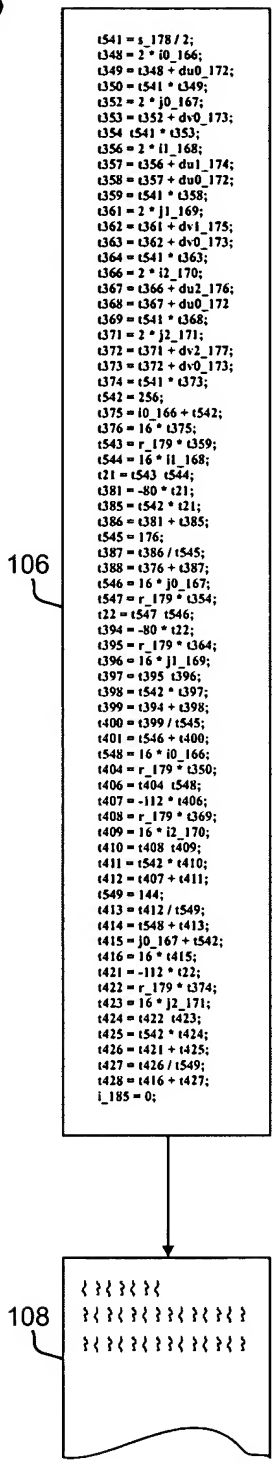


Fig. 2B

Fig. 3


t541 = s_178 / 2;
t348 = 2 * i0_166;
t349 = t348 + du0_172;
t350 = t541 * t349;
t352 = 2 * j0_167;
t353 = t352 + dv0_173;
t354 t541 * t353;
t356 = 2 * i1_168;
t357 = t356 + du1_174;
t358 = t357 + du0_172;
t359 = t541 * t358;
t361 = 2 * j1_169;
t362 = t361 + dv1_175;
t363 = t362 + dv0_173;
t364 = t541 * t363;
t366 = 2 * i2_170;
t367 = t366 + du2_176;
t368 = t367 + du0_172
t369 = t541 * t368;
t371 = 2 * j2_171;
t372 = t371 + dv2_177;
t373 = t372 + dv0_173;
t374 = t541 * t373;
t542 = 256;
t375 = i0_166 + t542;
t376 = 16 * t375;
t543 = r_179 * t359;
t544 = 16 * i1_168;
t21 = t543 t544;
t381 = -80 * t21;
t385 = t542 * t21;
t386 = t381 + t385;
t545 = 176;
t387 = t386 / t545;
t388 = t376 + t387;
t546 = 16 * j0_167;
t547 = r_179 * t354;
t22 = t547 t546;
t394 = -80 * t22;
t395 = r_179 * t364;
t396 = 16 * j1_169;
t397 = t395 t396;
t398 = t542 * t397;
t399 = t394 + t398;
t400 = t399 / t545;
t401 = t546 + t400;
t548 = 16 * i0_166;
t404 = r_179 * t350;
t406 = t404 t548;
t407 = -112 * t406;
t408 = r_179 * t369;
t409 = 16 * i2_170;
t410 = t408 t409;
t411 = t542 * t410;
t412 = t407 + t411;
t549 = 144;
t413 = t412 / t549;
t414 = t548 + t413;
t415 = j0_167 + t542;
t416 = 16 * t415;
t421 = -112 * t22;
t422 = r_179 * t374;
t423 = 16 * j2_171;
t424 = t422 t423;
t425 = t542 * t424;
t426 = t421 + t425;
t427 = t426 / t549;
t428 = t416 + t427;
i_185 = 0;
106
108

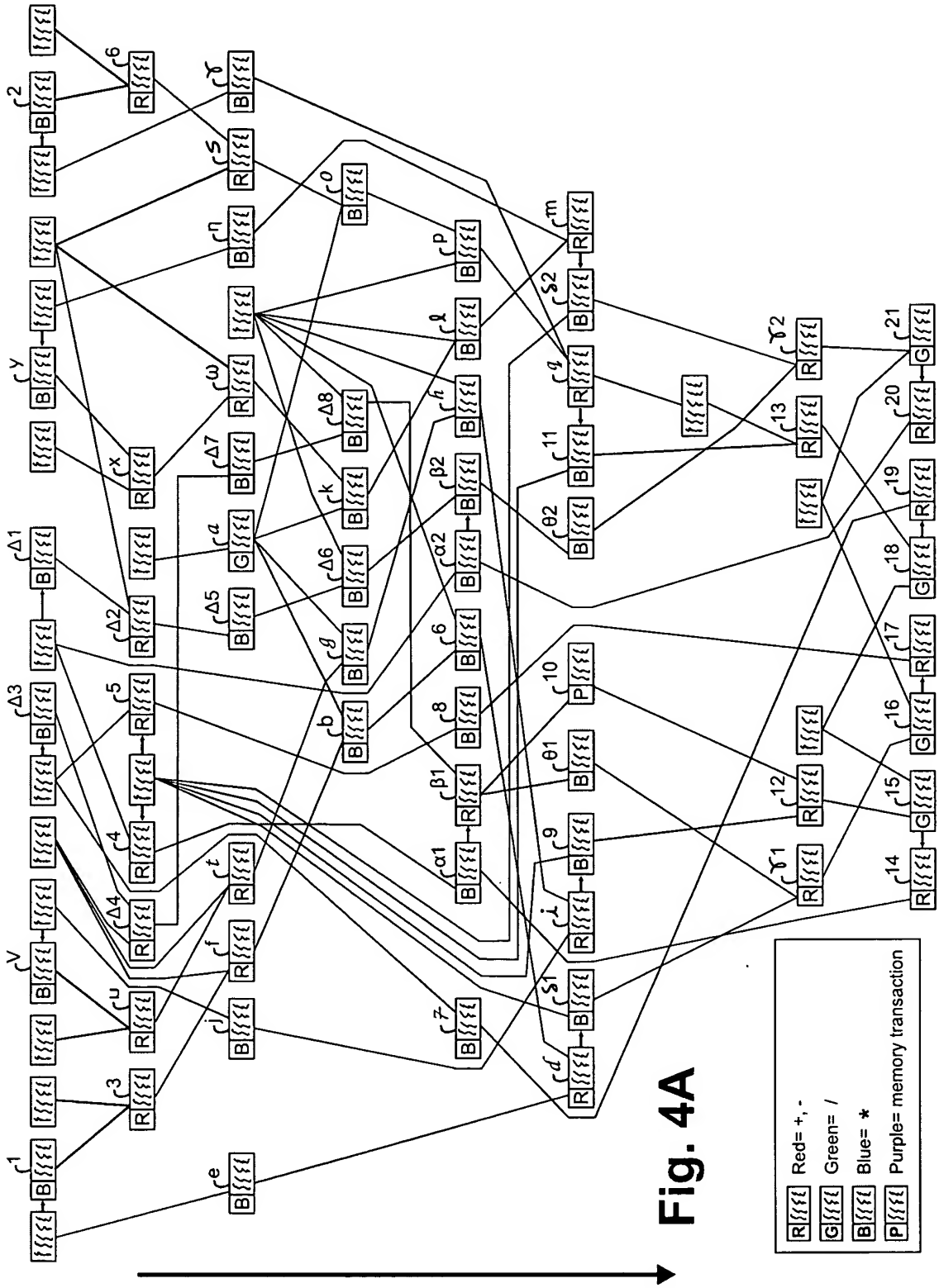


Fig. 4A

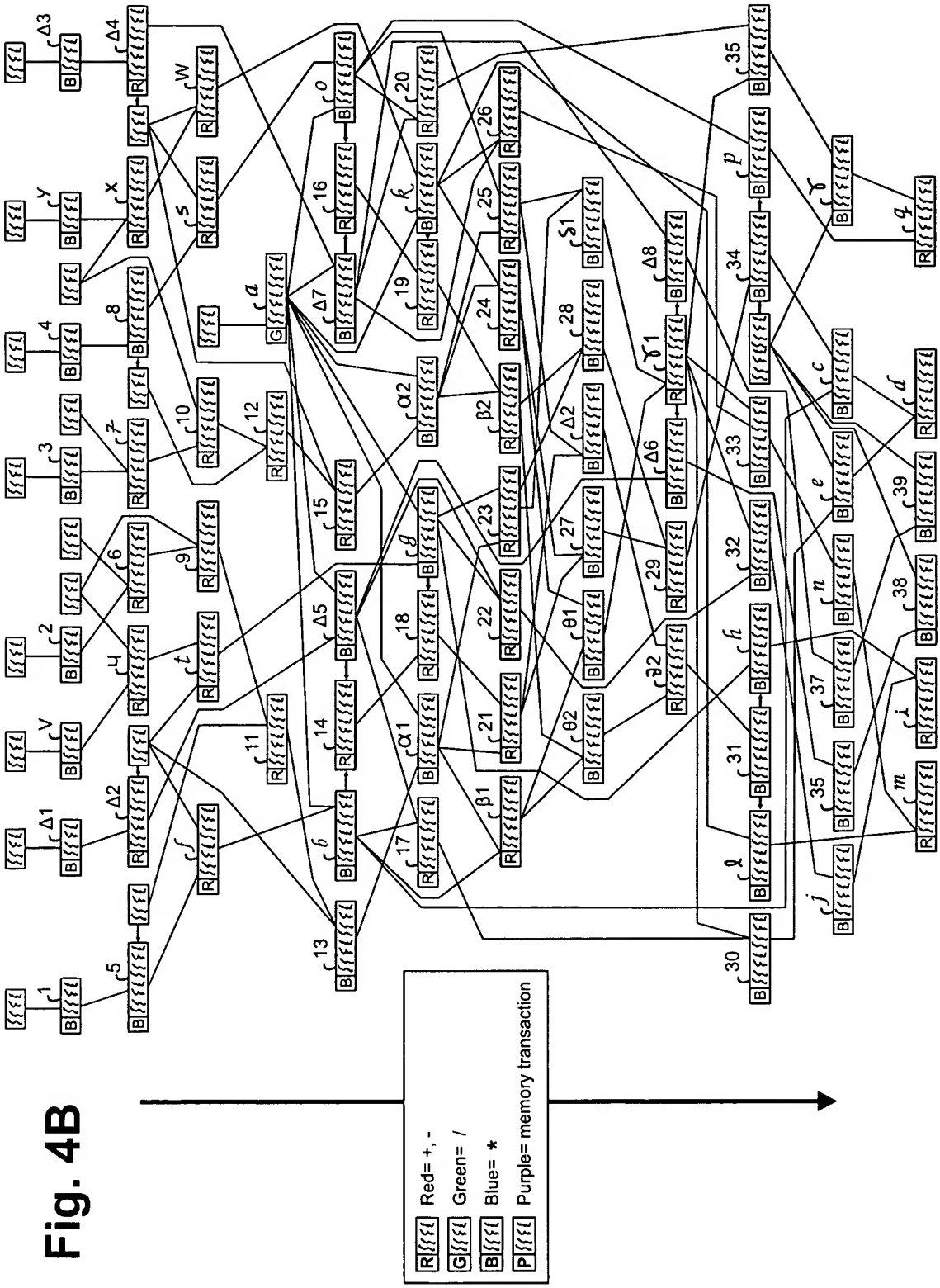


Fig. 4B

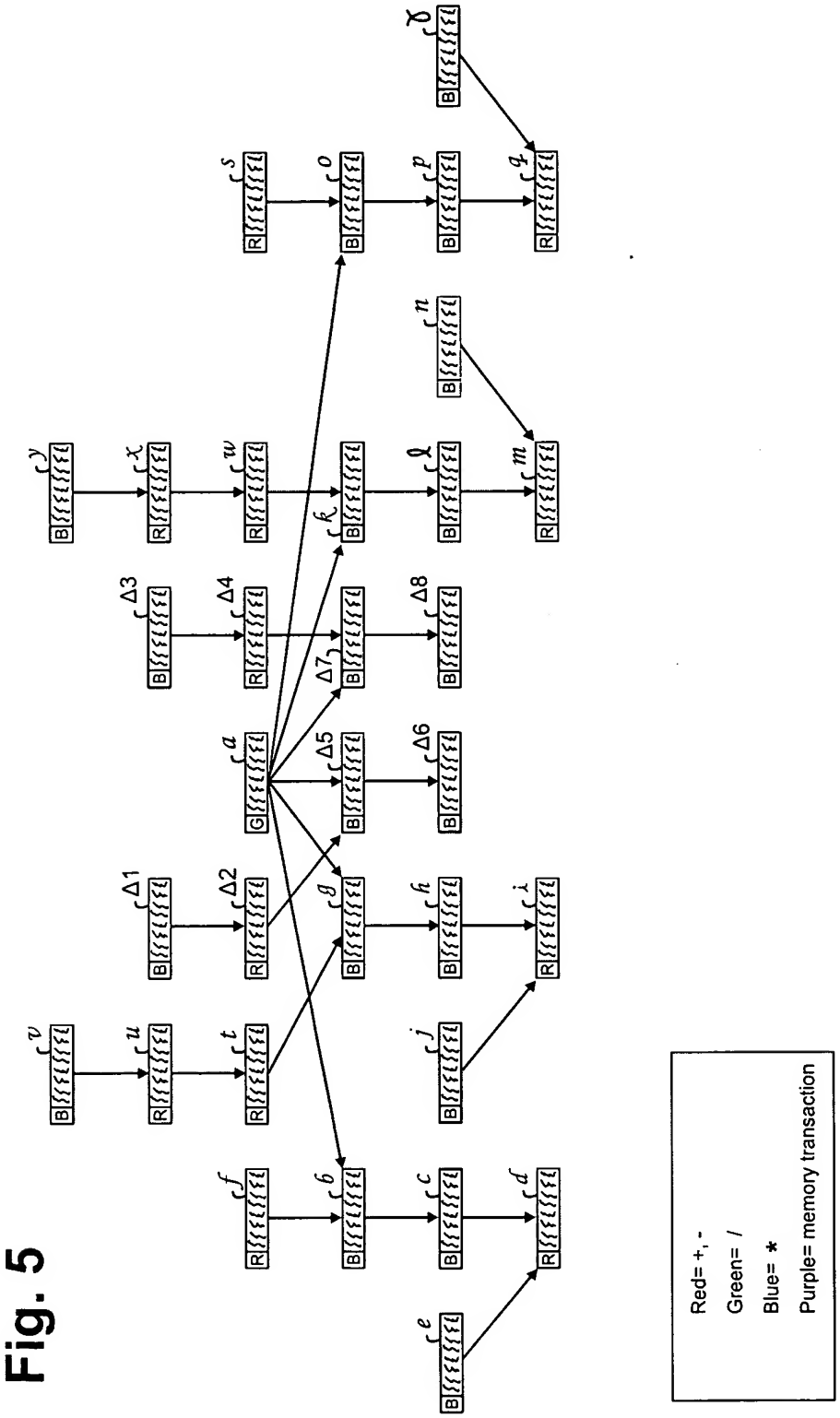


Fig. 5

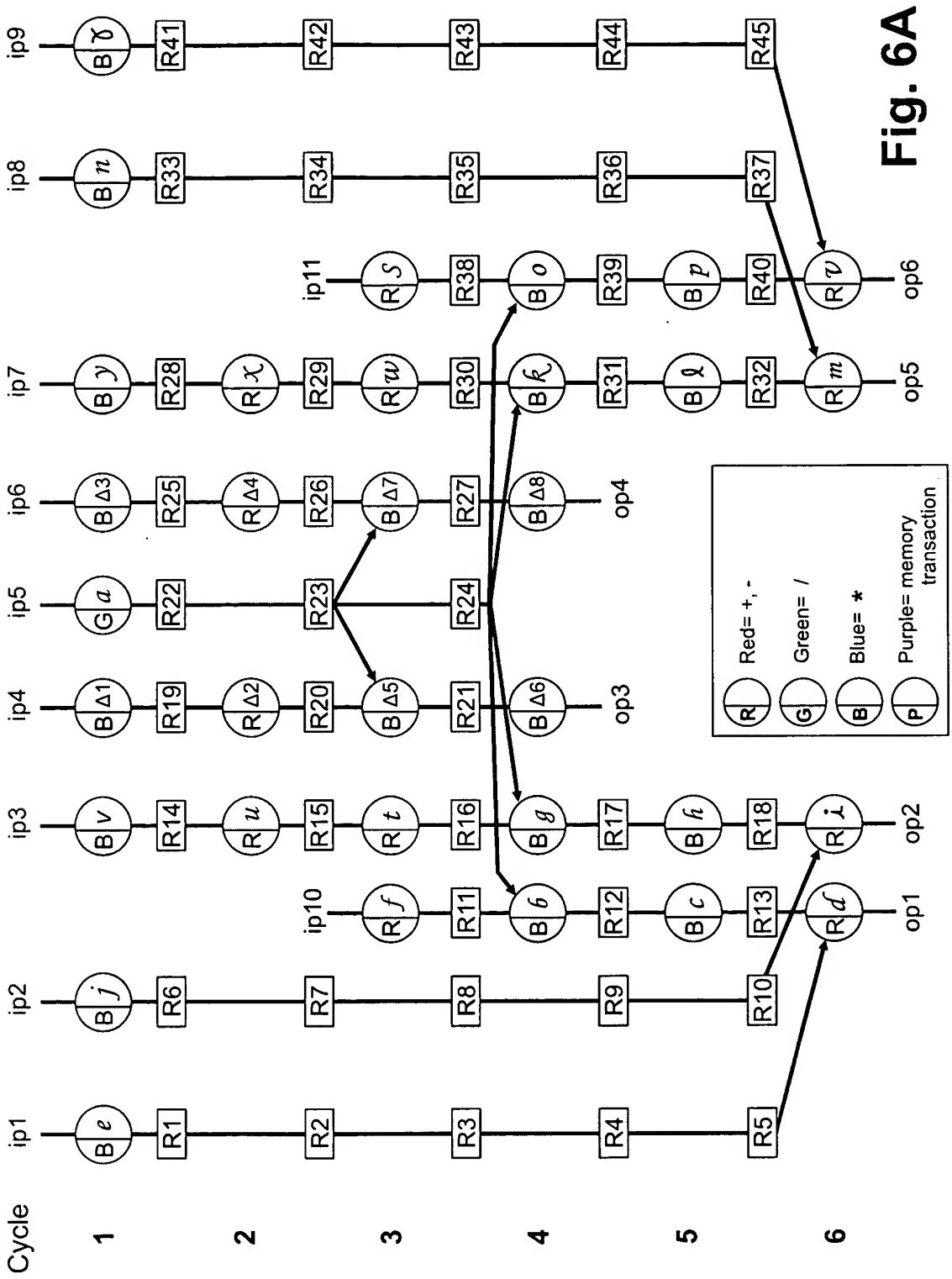

Cycle
1
2
3
4
5
6
ip1
ip2
ip3
ip4
ip5
ip6
ip7
ip8
ip9
ip10
ip11
op1
op2
op3
op4
op5
op6
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
Red= +, -
Green= /
Blue= *
Purple= memory transaction

Fig. 6A

Fig. 6B

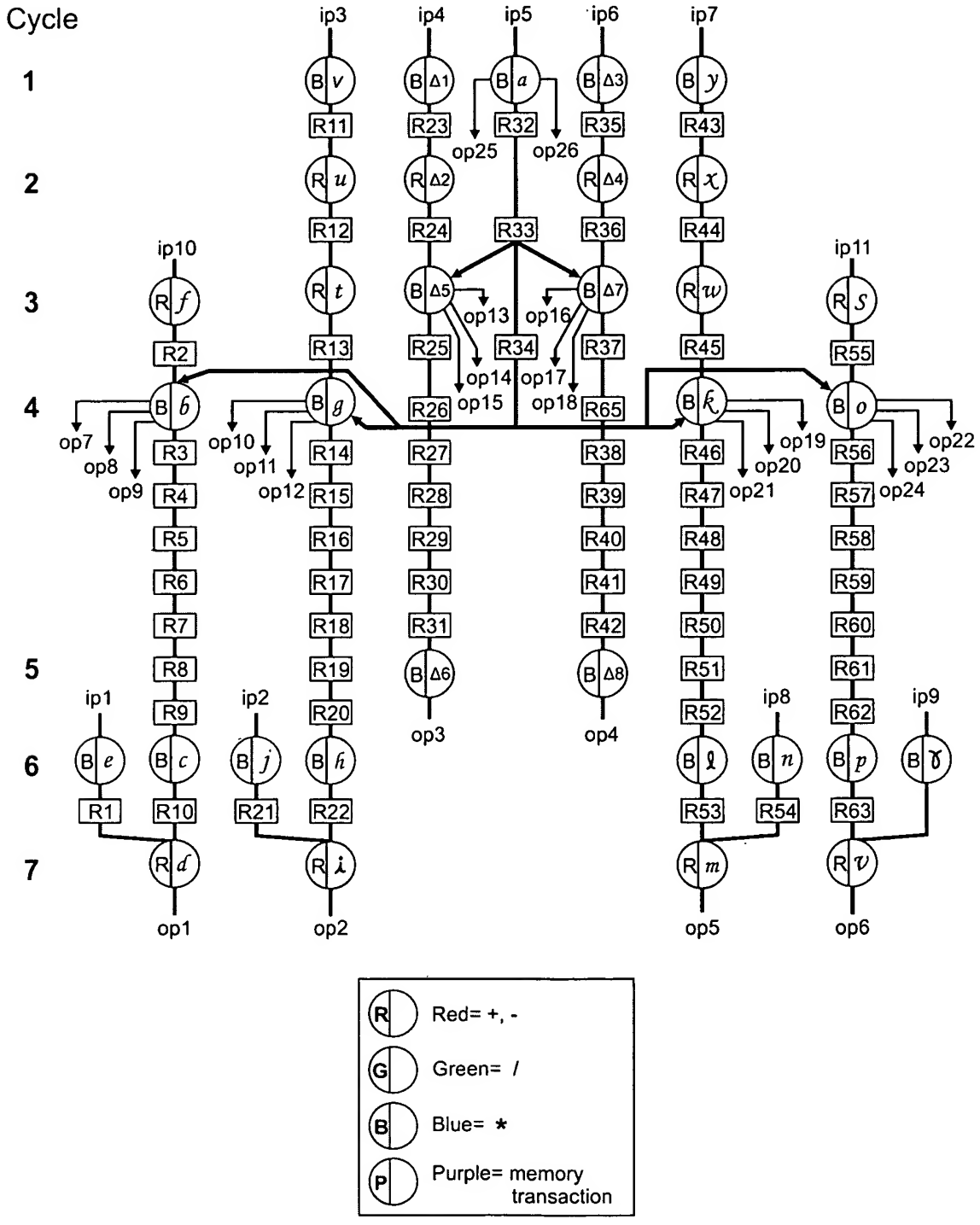

Cycle
1
2
3
4
5
6
7
ip1
ip2
ip3
ip4
ip5
ip6
ip7
ip8
ip9
ip10
ip11
op1
op2
op3
op4
op5
op6
op7
op8
op9
op10
op11
op12
op13
op14
op15
op16
op17
op18
op19
op20
op21
op22
op23
op24
op25
op26
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
R48
R49
R50
R51
R52
R53
R54
R55
R56
R57
R58
R59
R60
R61
R62
R63
R65
Red= +, -
Green= /
Blue= *
Purple= memory transaction

Fig. 7

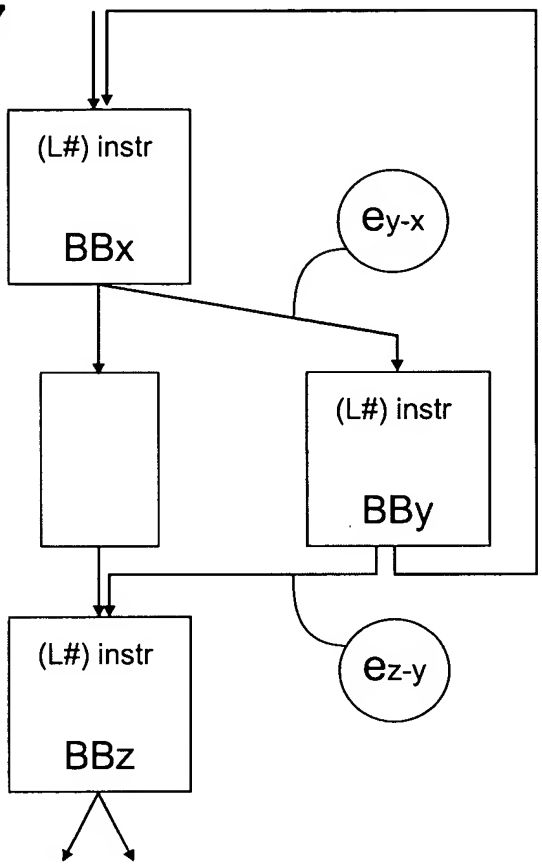


Fig. 8

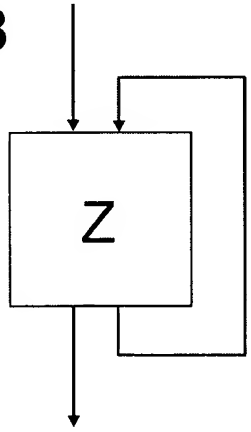


Fig. 9A

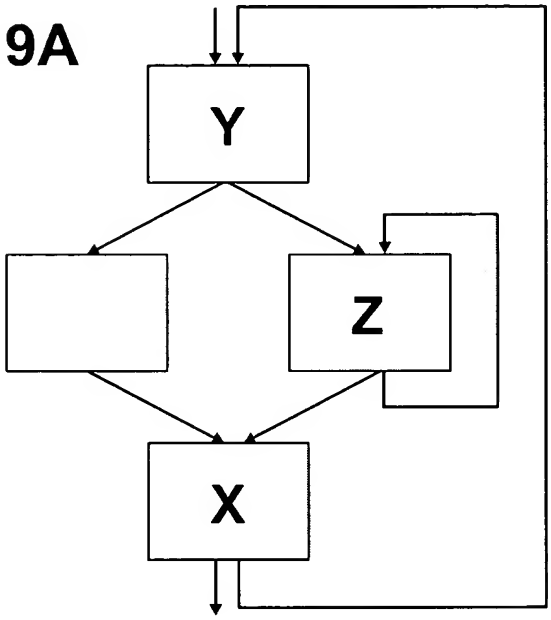


Fig. 9B

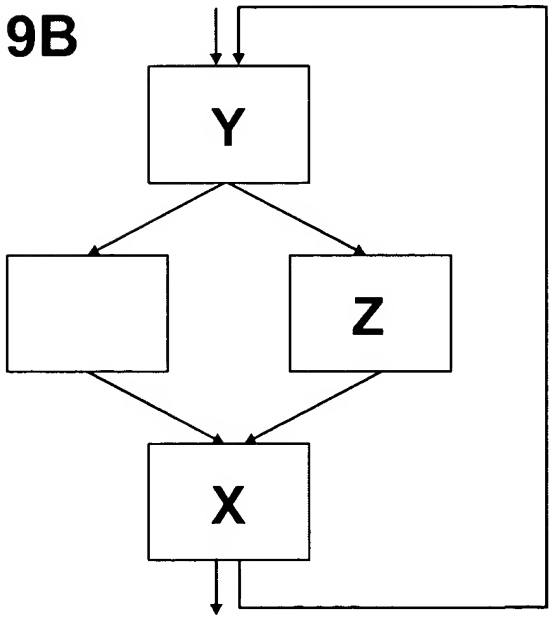


Fig. 10

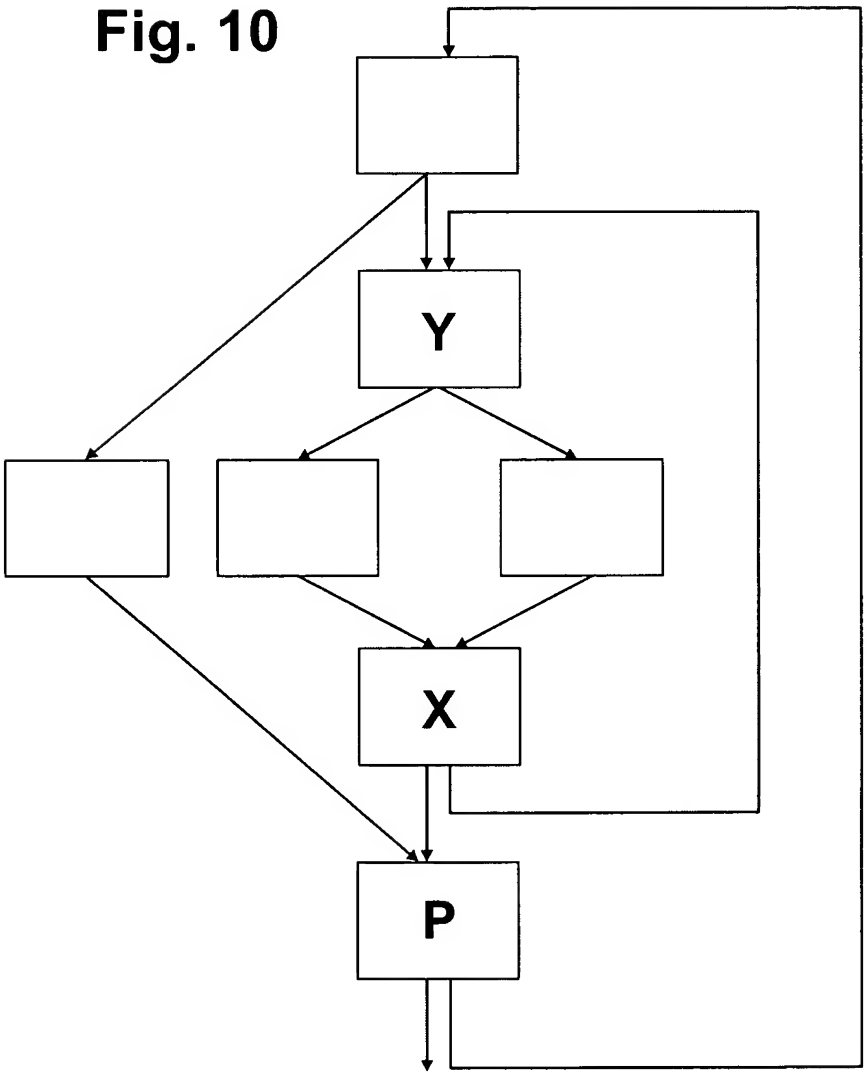


Fig. 11

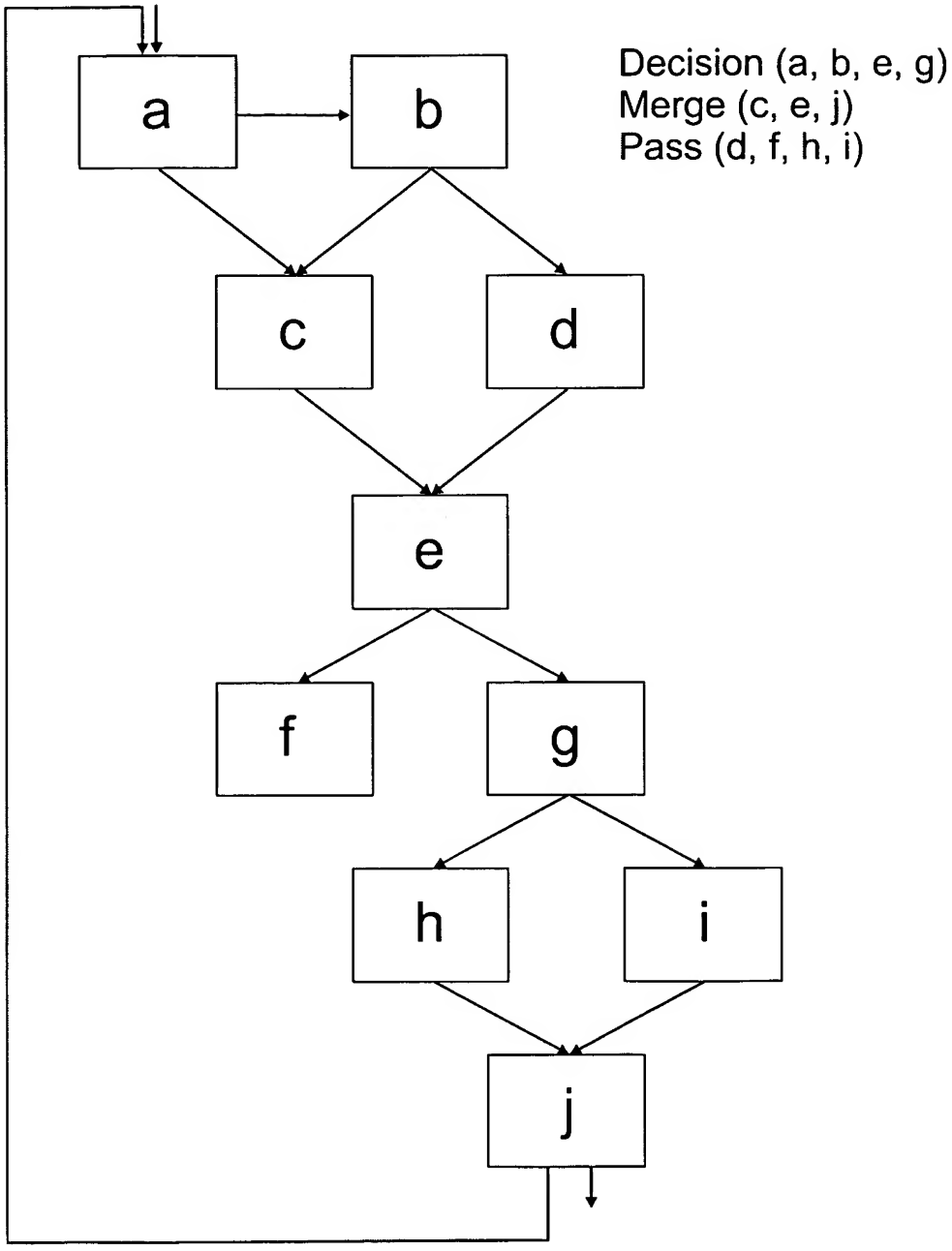


Fig. 12

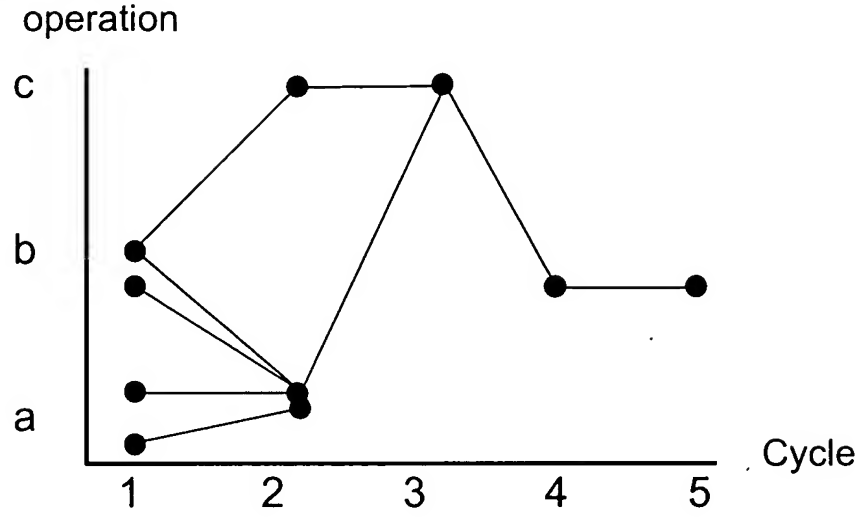


Fig. 12A

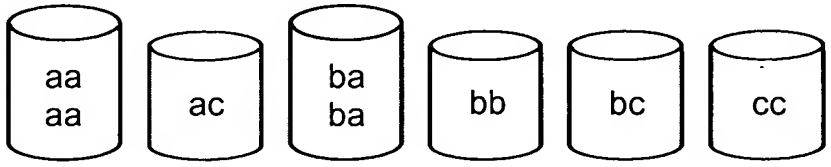


Fig. 13

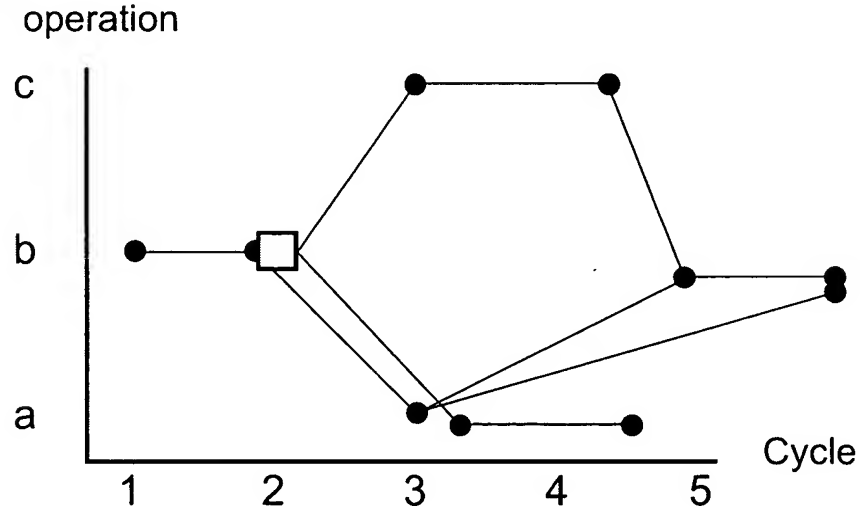


Fig. 13A

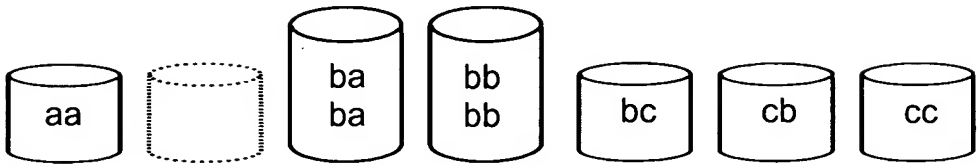


Fig. 14A

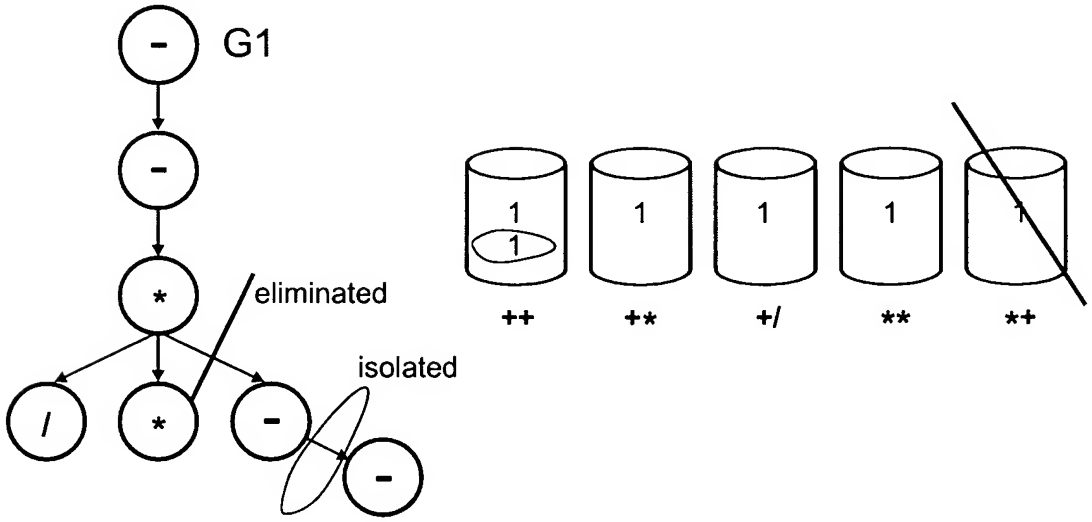


Fig. 14B

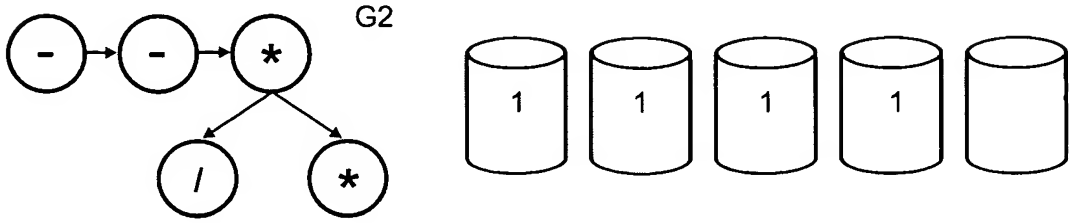


Fig. 15

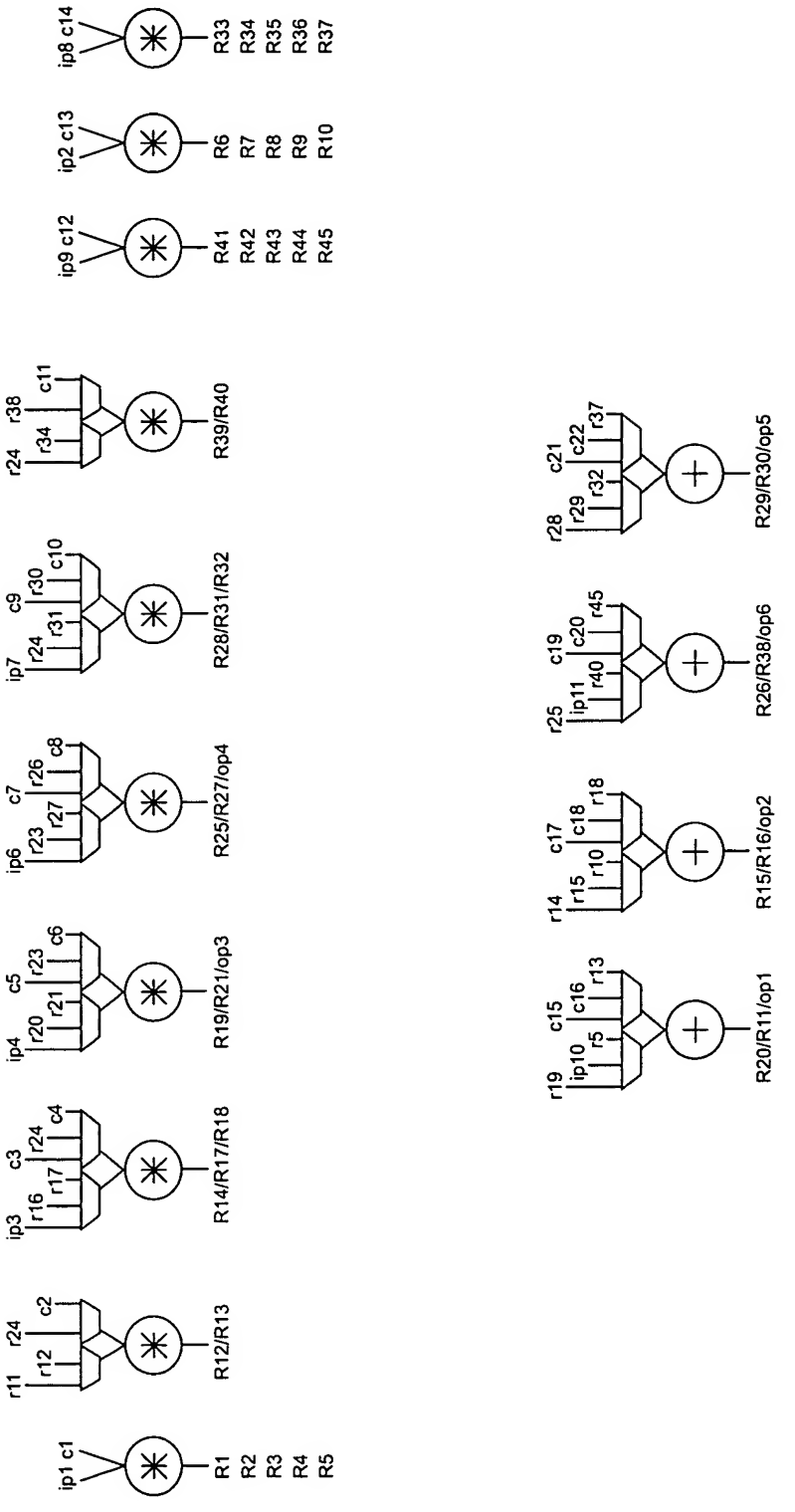

ip1 c1
r11 r24 c2
r12
r19 c15 c16 r13
ip10 r5
ip3 r16 c3 r24 c4
r17
r14 c17 c18 r18
r15 r10
ip4 r20 c5 r23 c6
r21
r25 c19 c20 r45
ip11 r40
ip6 r23 c7 r26 c8
r27
r28 c21 c22 r37
r29 r32
ip7 r24 c9 r30 c10
r31
r24 r34 r38 c11
ip9 c12
ip2 c13
ip8 c14
R1
R2
R3
R4
R5
R12/R13
R14/R17/R18
R19/R21/op3
R25/R27/op4
R28/R31/R32
R39/R40
R41
R42
R43
R44
R45
R6
R7
R8
R9
R10
R33
R34
R35
R36
R37
R20/R11/op1
R15/R16/op2
R26/R38/op6
R29/R30/op5

Fig. 16

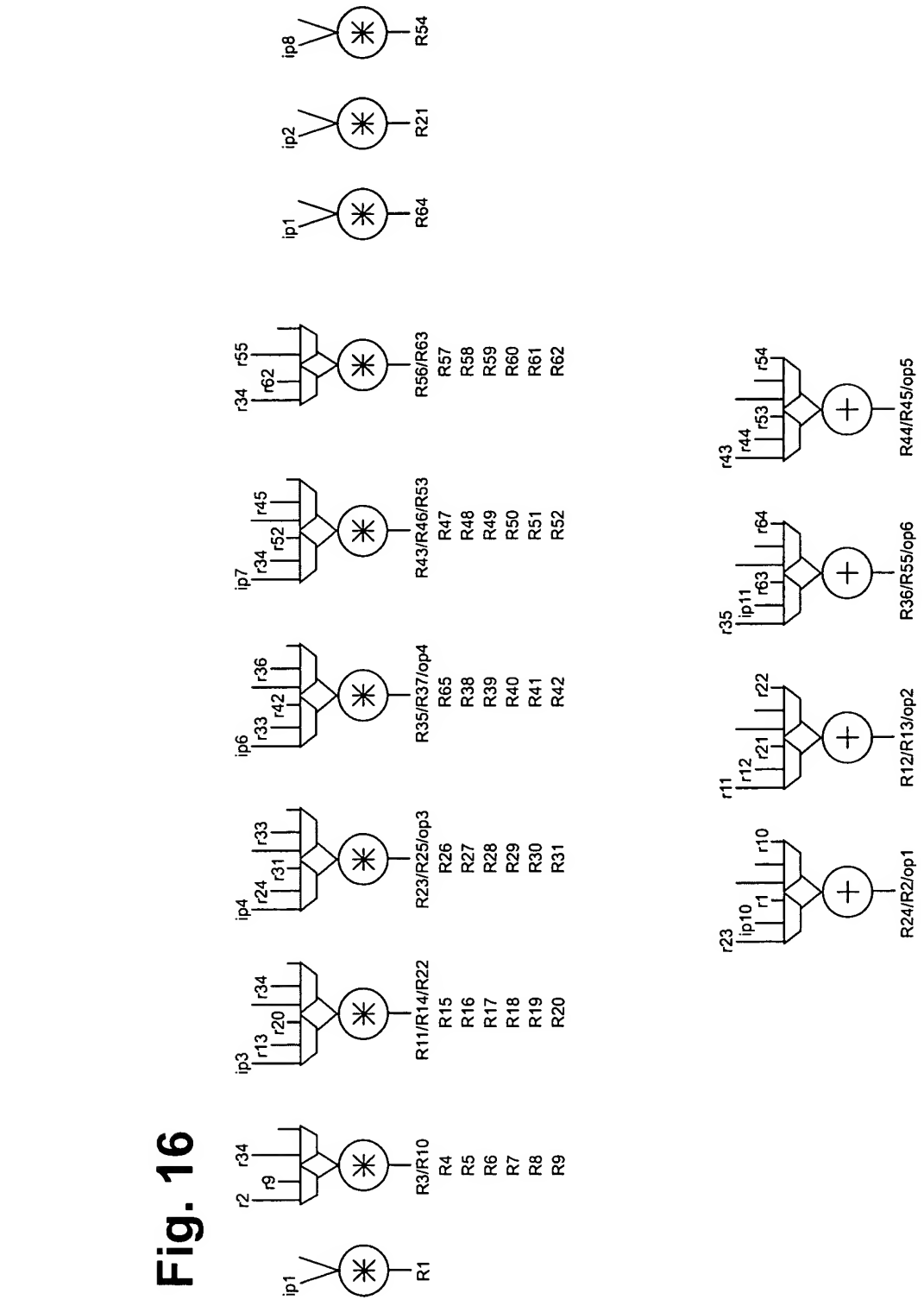

ip1
R1
r2
r34
r9
R3/R10
R4
R5
R6
R7
R8
R9
ip3
r13
r20
r34
R11/R14/R22
R15
R16
R17
R18
R19
R20
ip4
r24
r31
r33
R23/R25/op3
R26
R27
R28
R29
R30
R31
ip6
r33
r42
r36
R35/R37/op4
R65
R38
R39
R40
R41
R42
ip7
r34
r52
r45
R43/R46/R53
R47
R48
R49
R50
R51
R52
r34
r62
r55
R56/R63
R57
R58
R59
R60
R61
R62
ip1
R64
ip2
R21
ip8
R54
r23
ip10
r1
r10
R24/R2/op1
r11
r12
r21
r22
R12/R13/op2
r35
ip11
r63
r64
R36/R55/op6
r43
r44
r53
r54
R44/R45/op5

Fig. 17

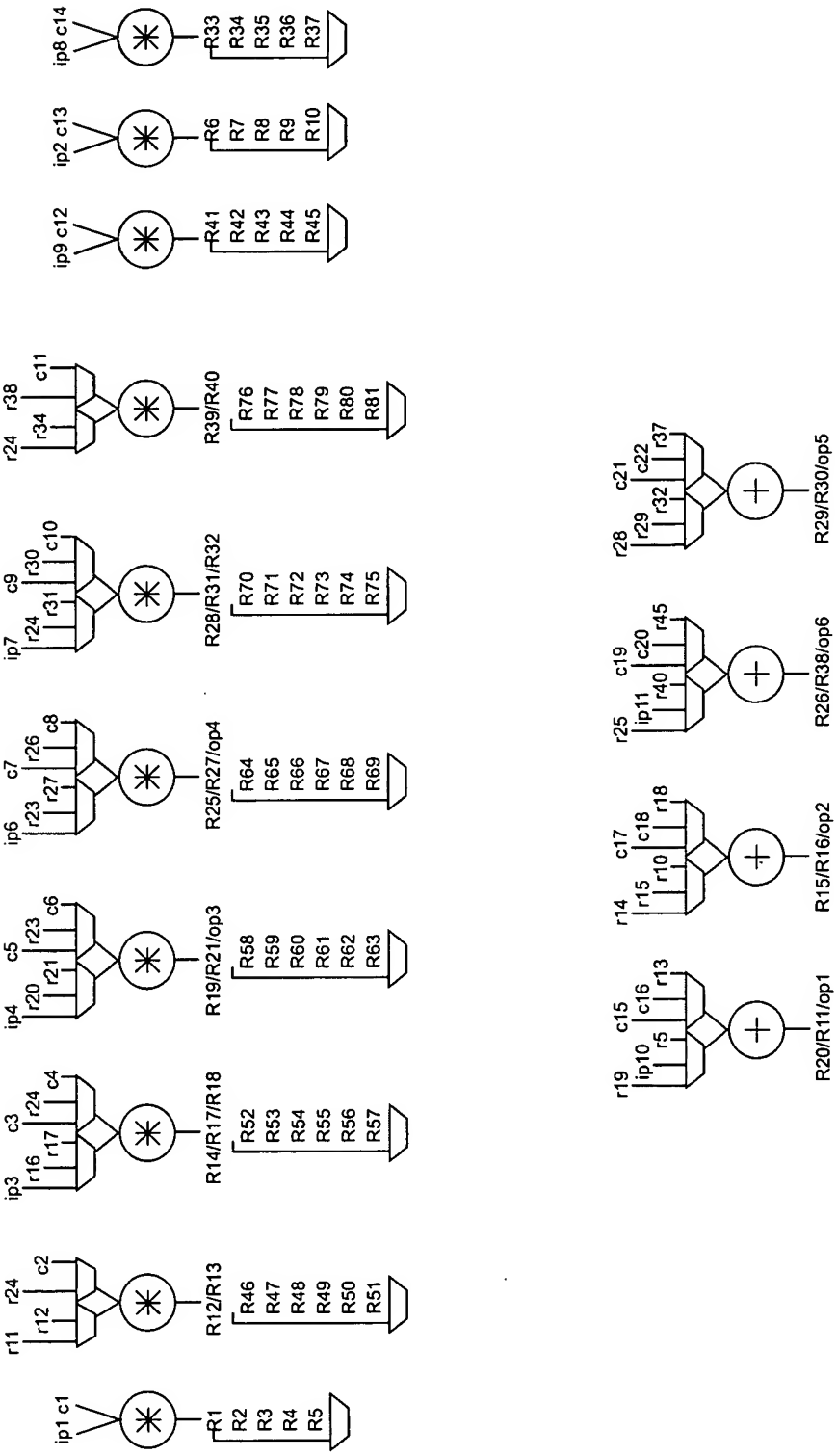

ip1 c1
R1
R2
R3
R4
R5
r11 r24 c2
r12
R12/R13
R46
R47
R48
R49
R50
R51
ip3 c3 r24 c4
r16 r17
R14/R17/R18
R52
R53
R54
R55
R56
R57
ip4 c5 r23 c6
r20 r21
R19/R21/op3
R58
R59
R60
R61
R62
R63
ip6 c7 r26 c8
r23 r27
R25/R27/op4
R64
R65
R66
R67
R68
R69
ip7 c9 r30 c10
r24 r31
R28/R31/R32
R70
R71
R72
R73
R74
R75
r24 r38 c11
r34
R39/R40
R76
R77
R78
R79
R80
R81
ip9 c12
R41
R42
R43
R44
R45
ip2 c13
R6
R7
R8
R9
R10
ip8 c14
R33
R34
R35
R36
R37
r19 ip10 c15 r5 c16 r13
R20/R11/op1
r14 r15 c17 r10 c18 r18
R15/R16/op2
r25 ip11 c19 r40 c20 r45
R26/R38/op6
r28 r29 c21 r32 c22 r37
R29/R30/op5

Fig. 18

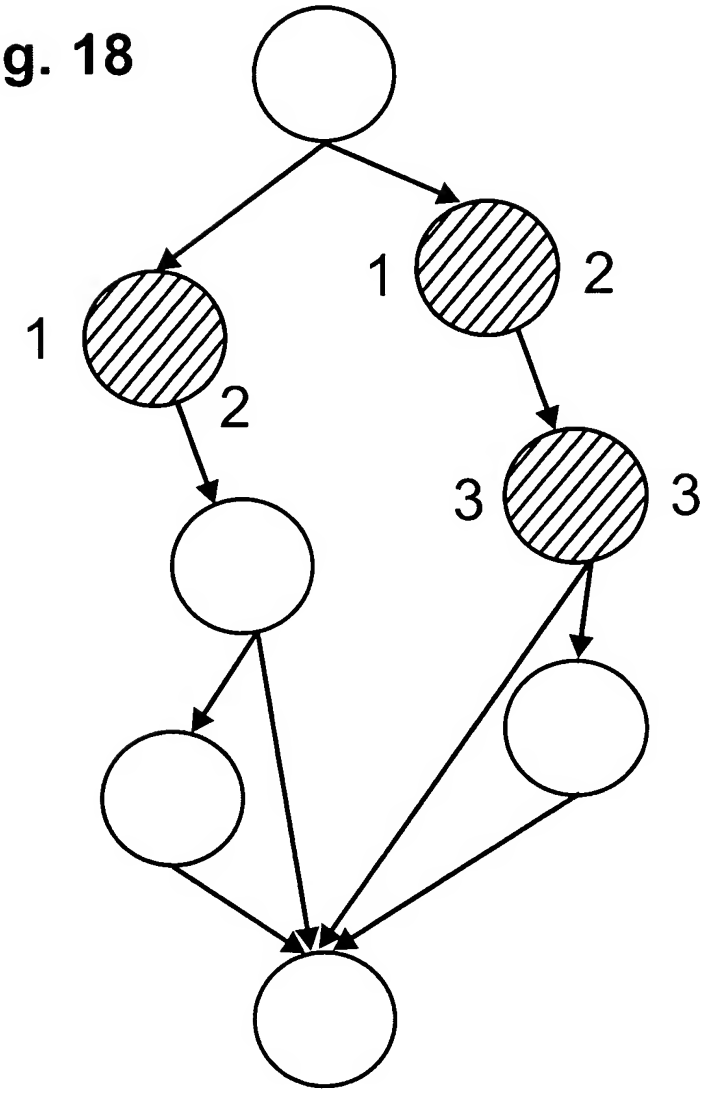


Fig. 19

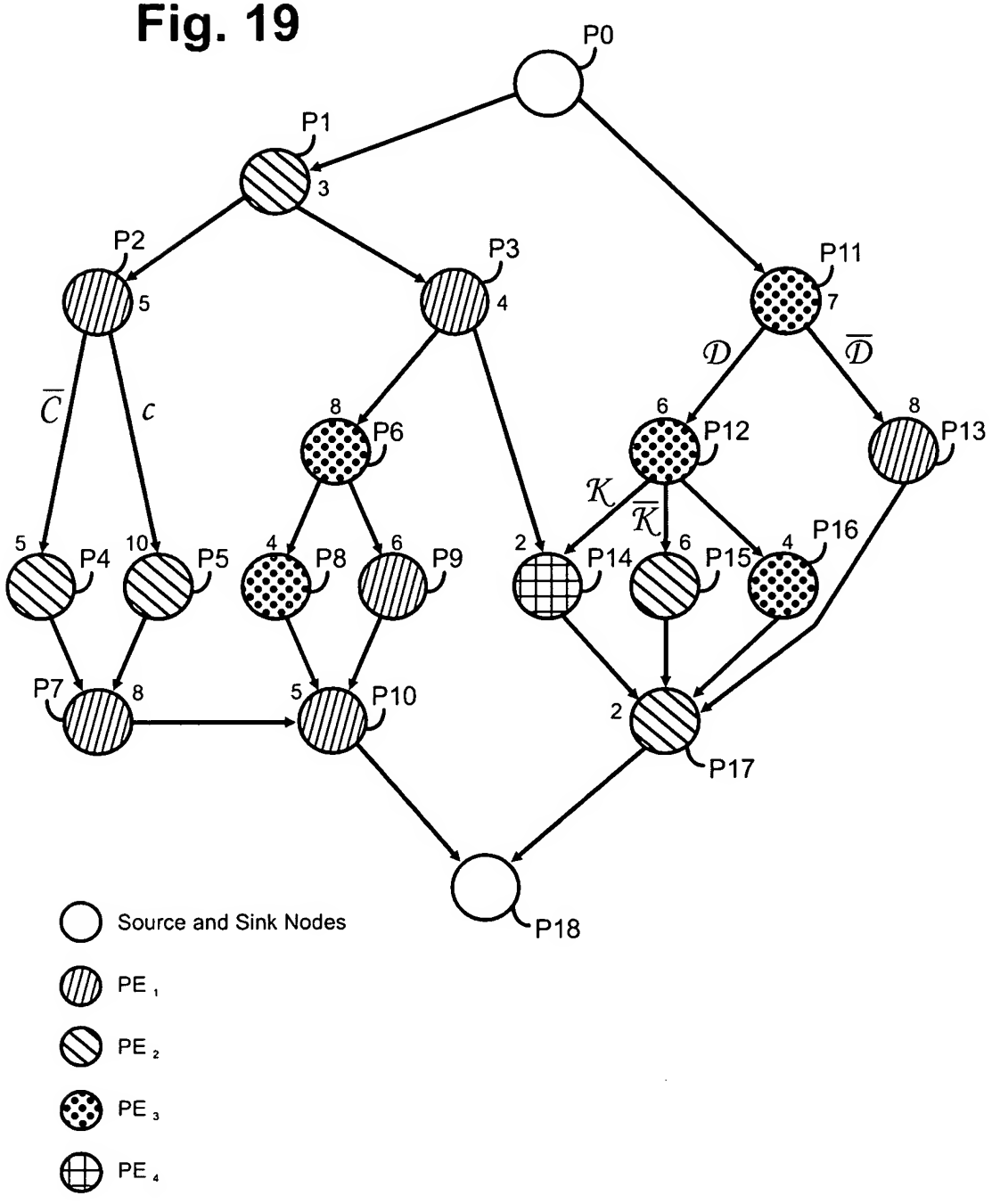

P0
P1
3
P2
5
P3
4
P11
7
$\overline{C}$
C
$\mathcal{D}$
$\overline{\mathcal{D}}$
8
P6
6
P12
8
P13
$\mathcal{K}$
$\overline{\mathcal{K}}$
5
P4
10
P5
4
P8
6
P9
2
P14
6
P15
4
P16
P7
8
5
P10
2
P17
P18
Source and Sink Nodes
PE 1
PE 2
PE 3
PE 4

Fig. 20

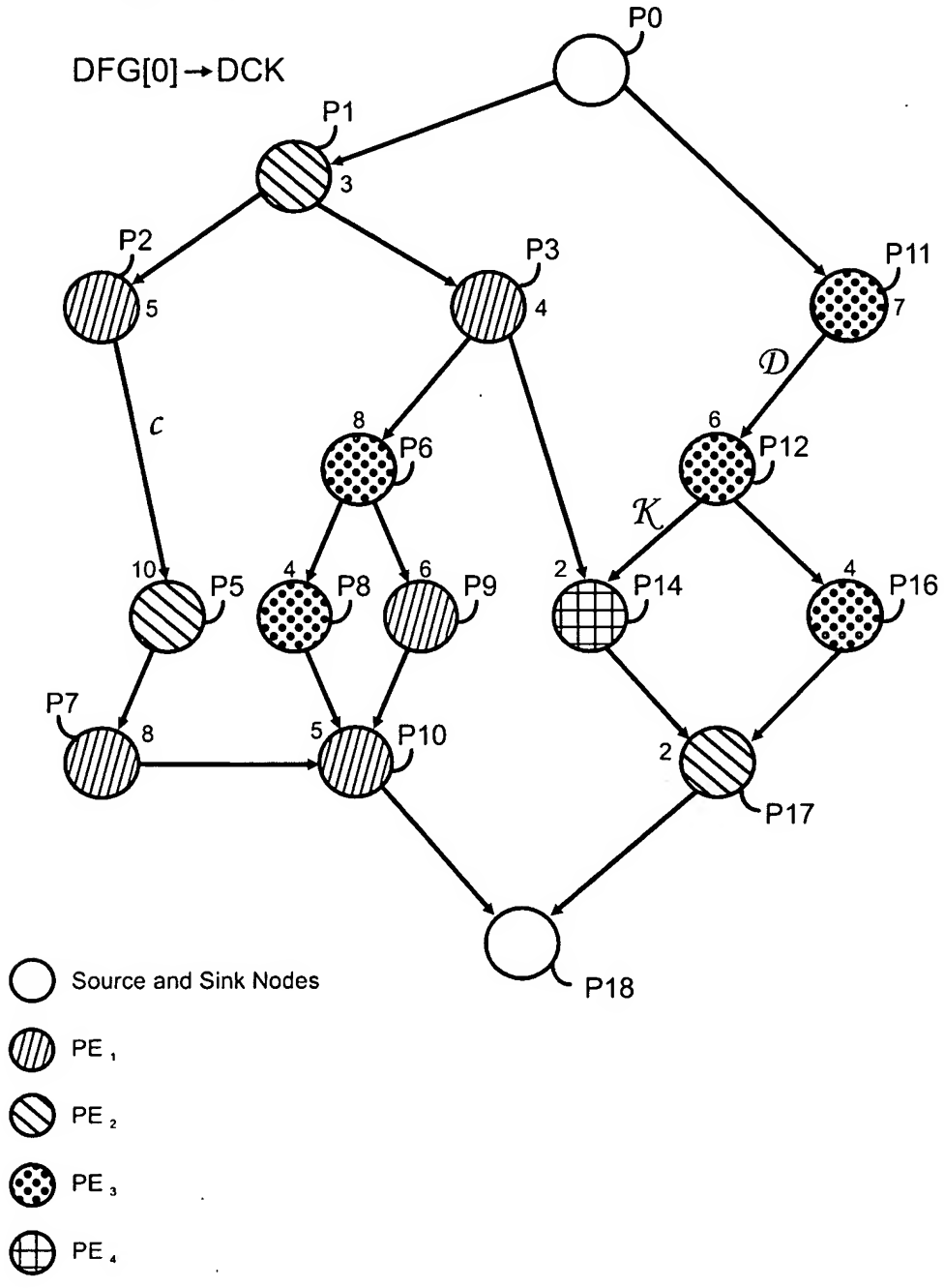

DFG[0]→DCK
P0
P1
3
P2
5
P3
4
P11
7
C
D
8
P6
6
P12
K
10
P5
4
P8
6
P9
2
P14
4
P16
P7
8
5
P10
2
P17
P18
Source and Sink Nodes
PE1
PE2
PE3
PE4

Fig. 21

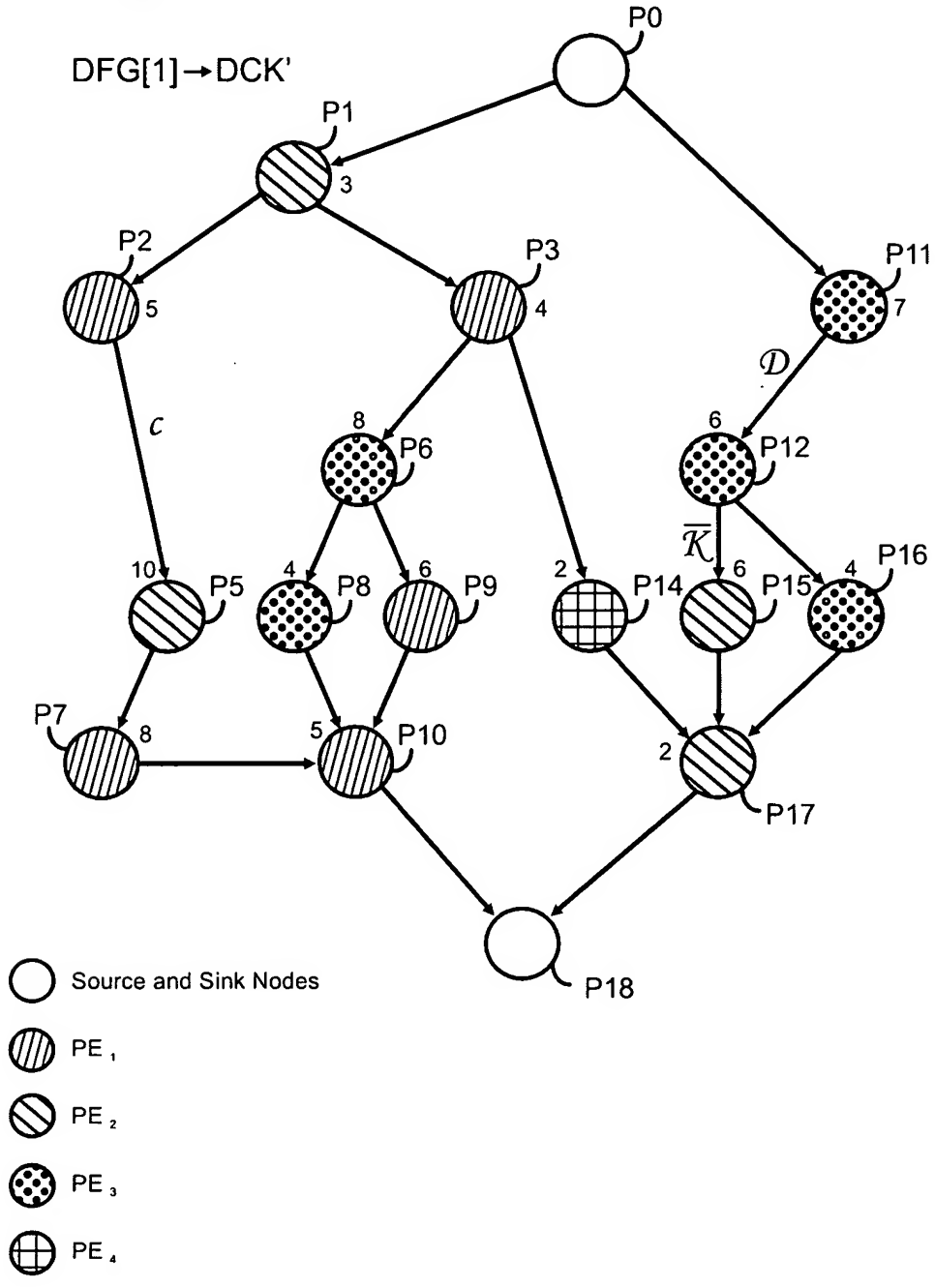

DFG[1]→DCK'
P0
P1
3
P2
5
P3
4
P11
7
D
C
8
P6
6
P12
K
10
P5
4
P8
6
P9
2
P14
6
P15
4
P16
P7
8
5
P10
2
P17
P18
Source and Sink Nodes
PE 1
PE 2
PE 3
PE 4

Fig. 22

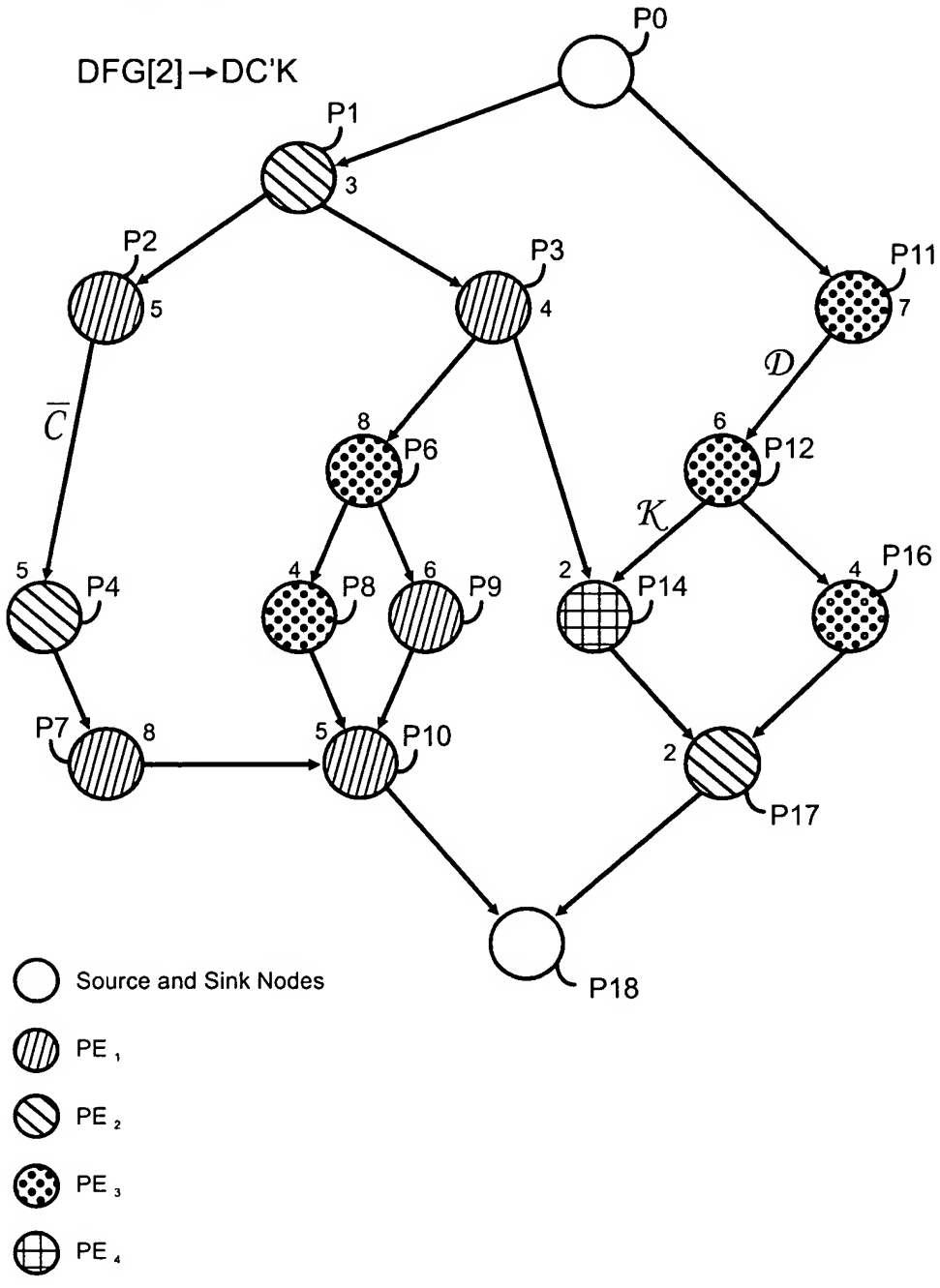

DFG[2]→DC'K
P0
P1
3
P2
5
P3
4
P11
7
$\overline{C}$
$\mathcal{D}$
8
P6
6
P12
$\mathcal{K}$
5
P4
4
P8
6
P9
2
P14
4
P16
P7
8
5
P10
2
P17
P18
Source and Sink Nodes
PE 1
PE 2
PE 3
PE 4

Fig. 23

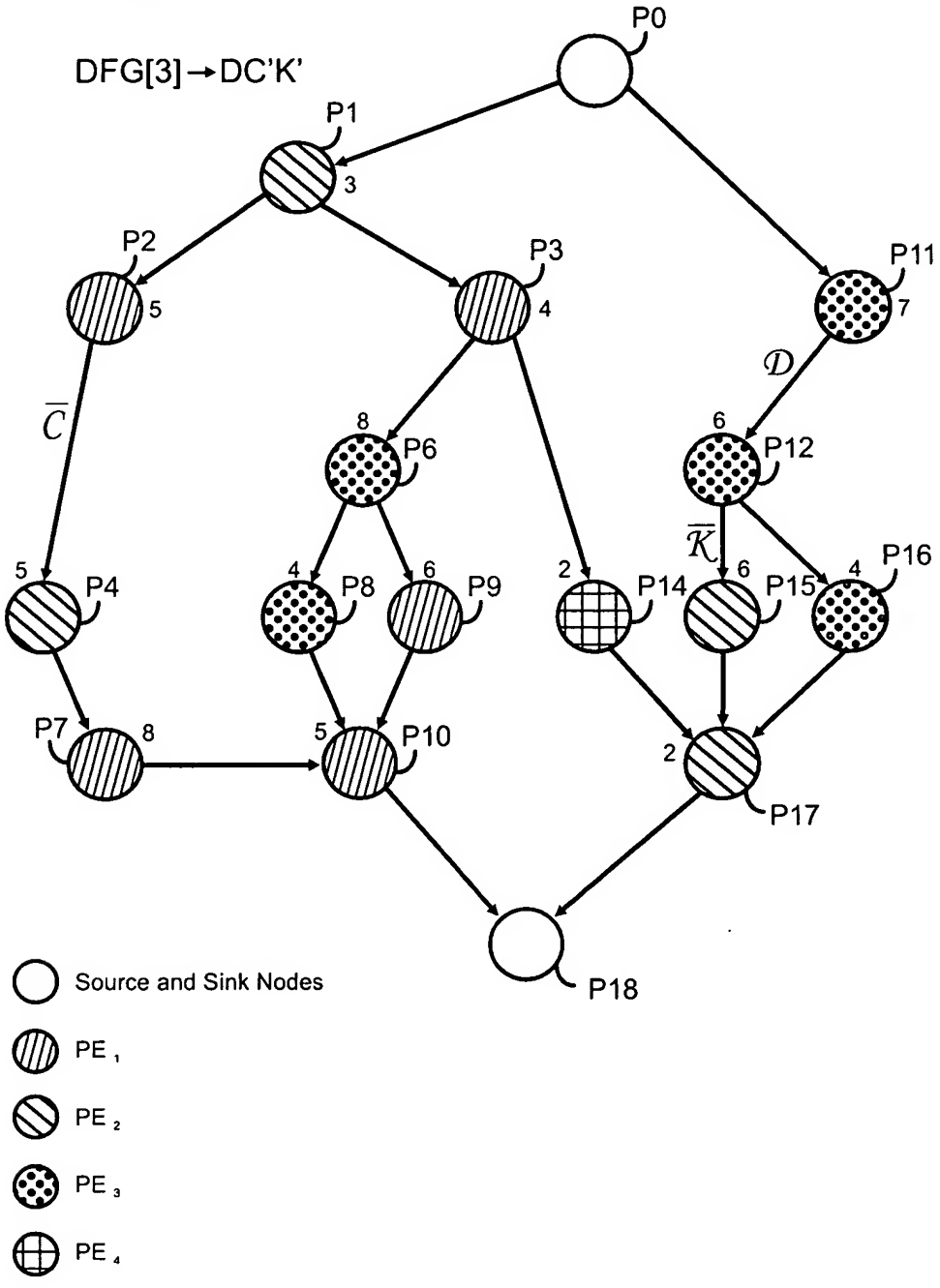

DFG[3]→DC'K'
P0
P1
3
P2
5
P3
4
P11
7
$\overline{C}$
$\mathcal{D}$
8
P6
6
P12
$\overline{\mathcal{K}}$
5
P4
4
P8
6
P9
2
P14
6
P15
4
P16
P7
8
5
P10
2
P17
P18
Source and Sink Nodes
PE 1
PE 2
PE 3
PE 4

Fig. 24

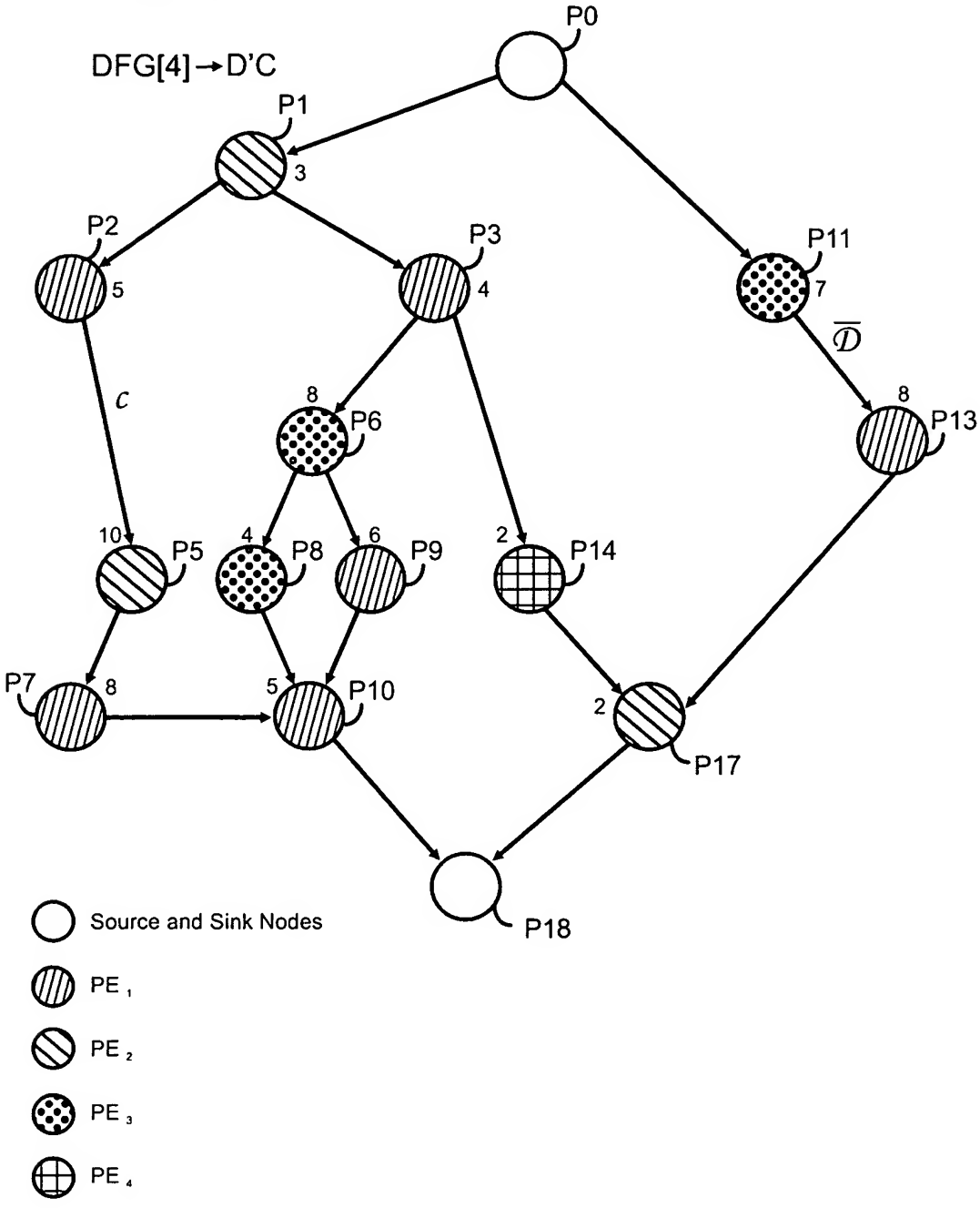

DFG[4]→D'C
P0
P1
3
P2
5
P3
4
P11
7
$\overline{D}$
C
8
P6
8
P13
10
P5
4
P8
6
P9
2
P14
P7
8
5
P10
2
P17
P18
Source and Sink Nodes
PE 1
PE 2
PE 3
PE 4

Fig. 25

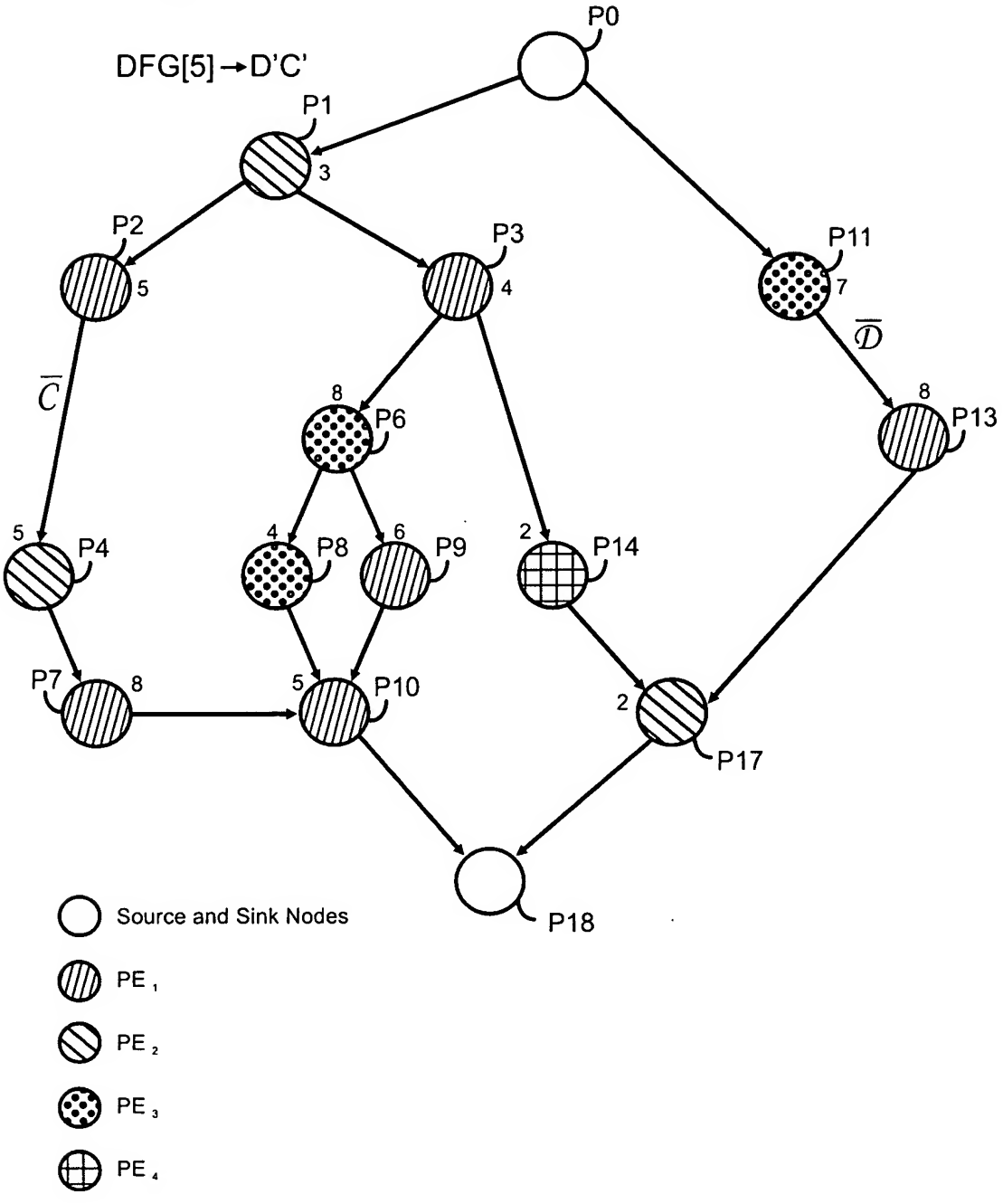

DFG[5]→D'C'
P0
P1
3
P2
5
P3
4
P11
7
$\overline{D}$
$\overline{C}$
8
P6
8
P13
5
P4
4
P8
6
P9
2
P14
P7
8
5
P10
2
P17
P18
Source and Sink Nodes
PE 1
PE 2
PE 3
PE 4

Fig. 26

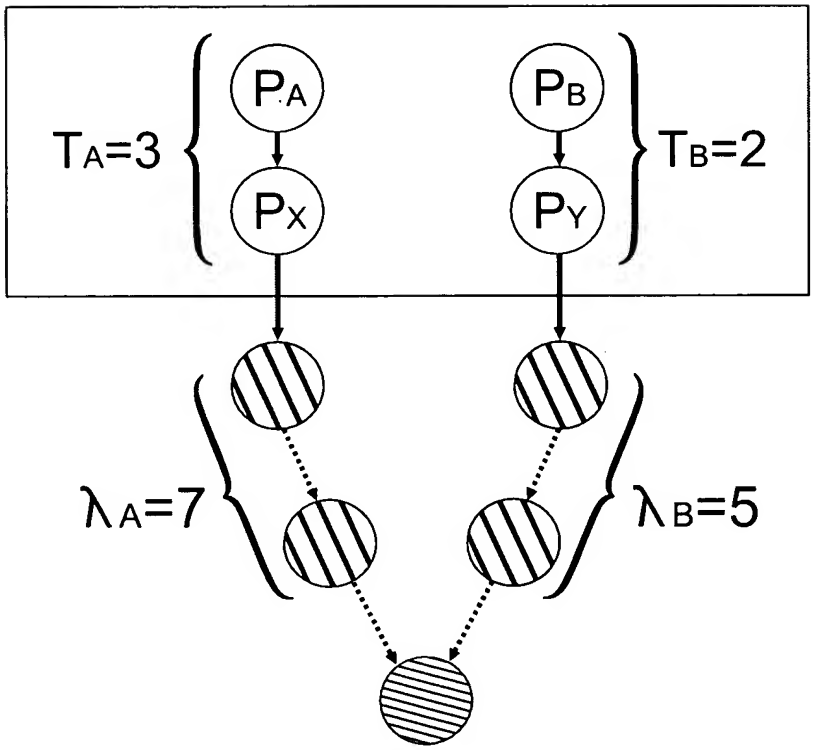


Fig. 27

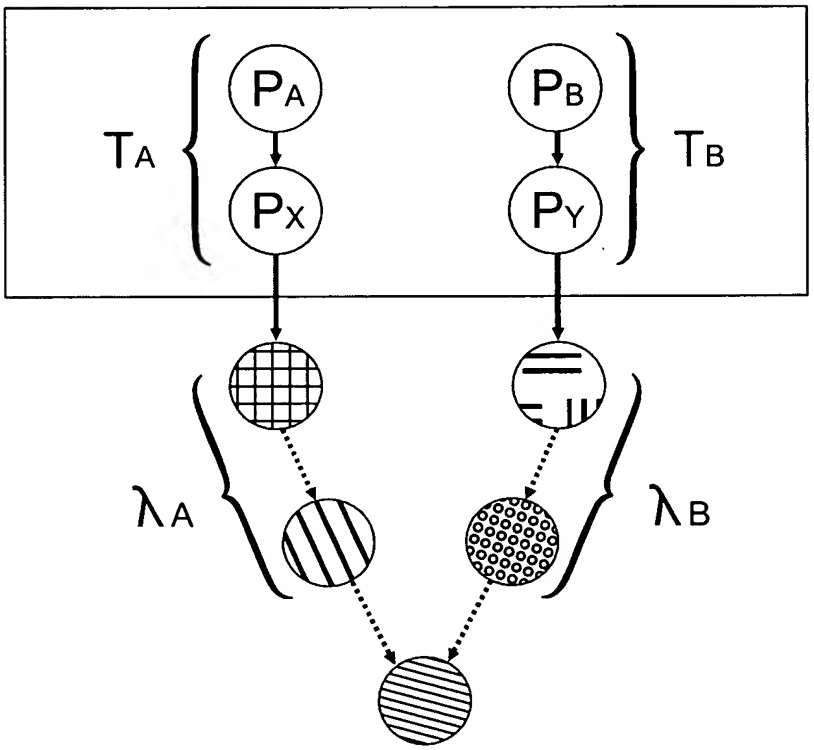


Fig. 28

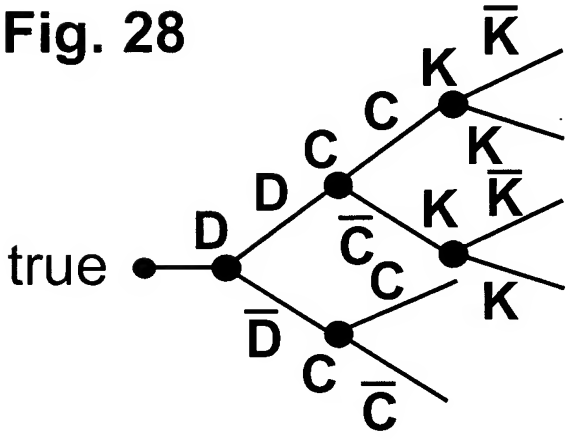


Fig. 29A

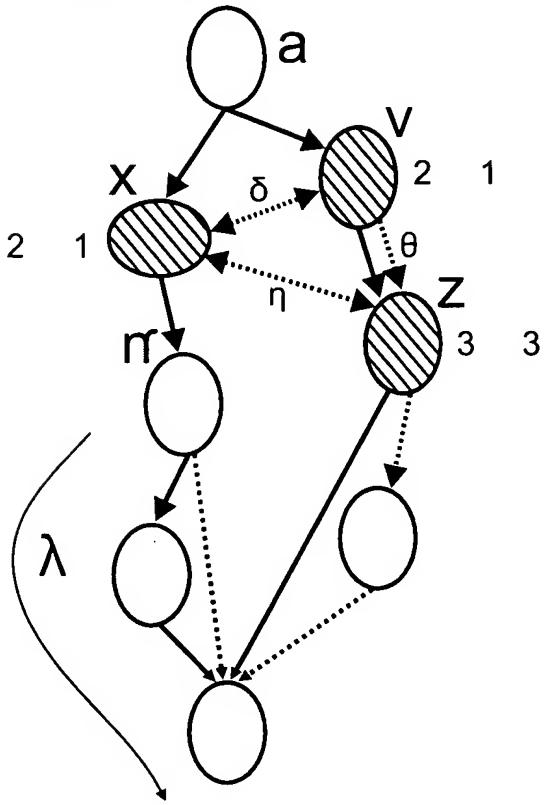
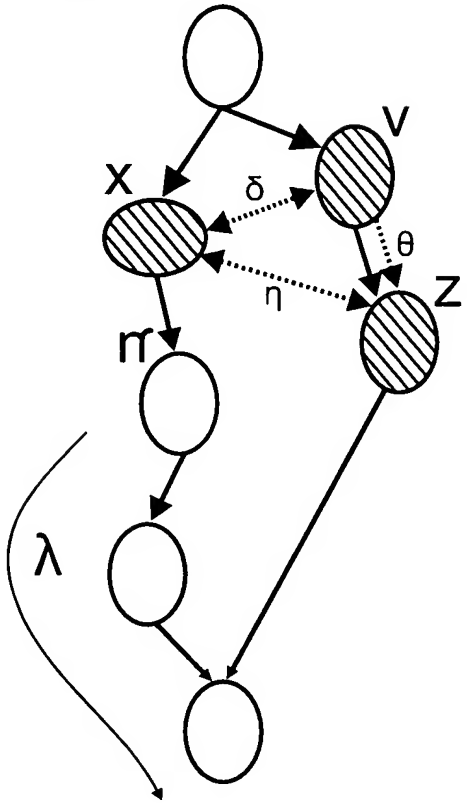
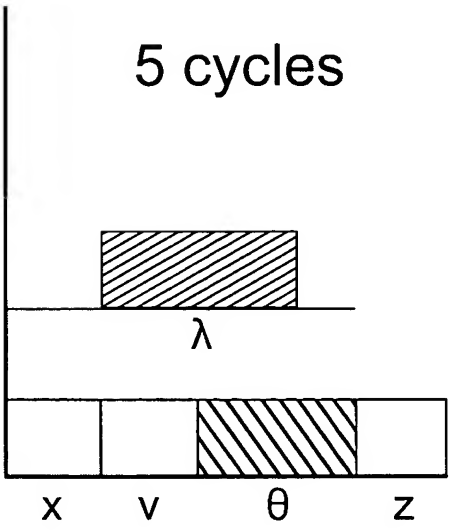


Fig. 29B





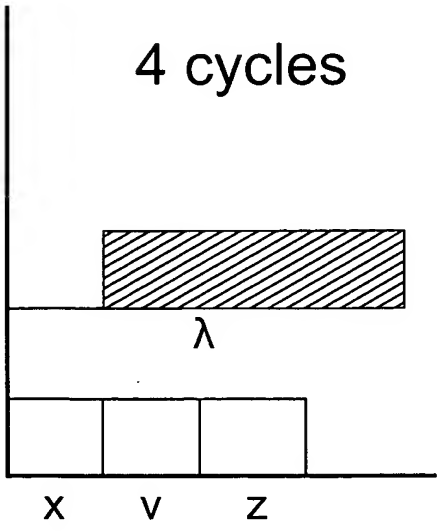


Fig. 30

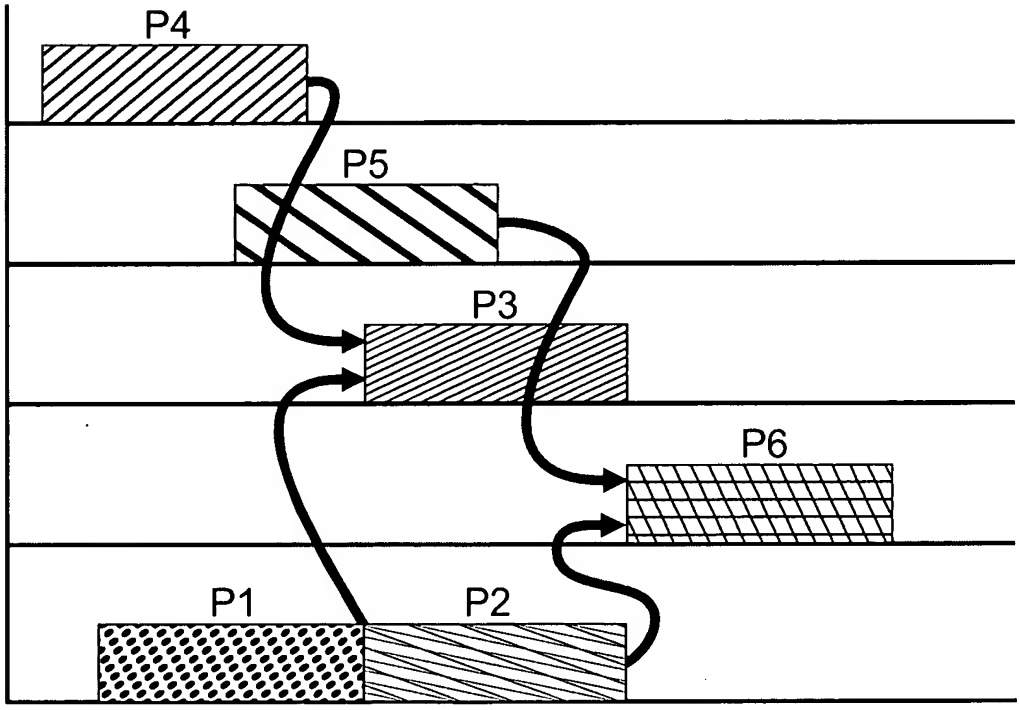


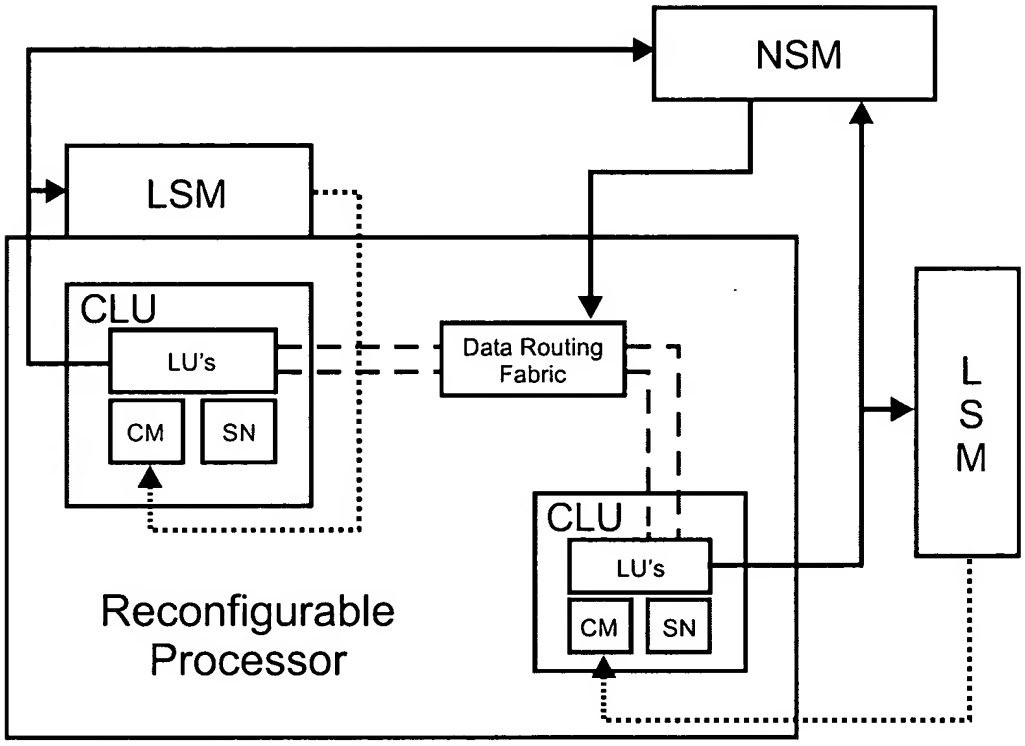
Fig. 31

	Expression α	Expression β	Expression θ	Expression ϒ
Process A		0		
Process B		10		
.....				
.....				

	Expression α	Expression β	Expression θ	Expression ϒ
Process A		30		
Process B		40		
.....				
.....				

↓ .....
and so on

Fig. 32



CLU=Configurable Logic Unit
LU=Logic Units
SN=Switching Network
CM=Configuration Memory
LSM=Logic Schedule Manager
NSM=Network Schedule Manager

Fig. 33

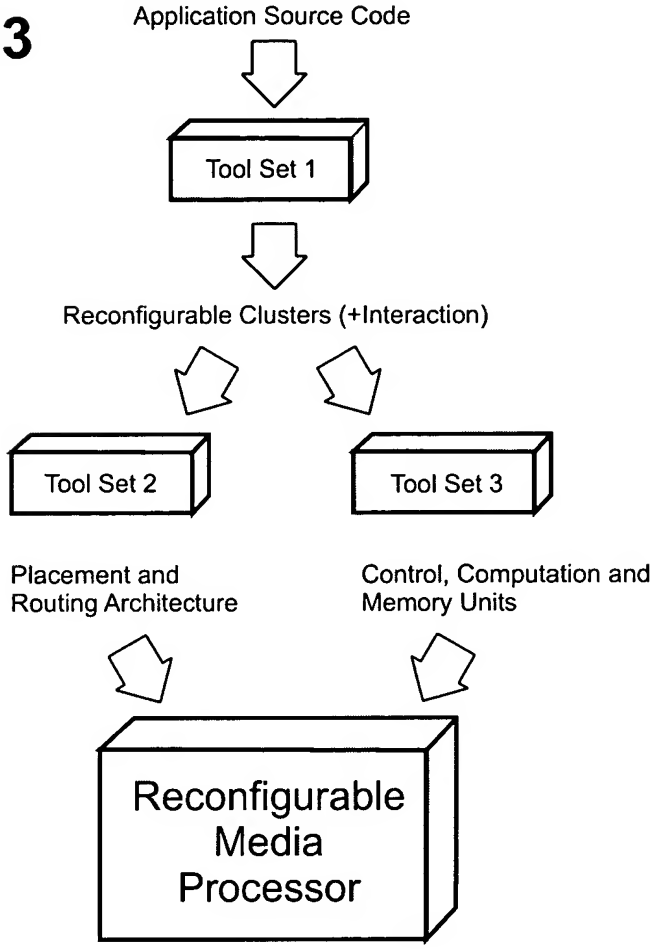

Application Source Code
Tool Set 1
Reconfigurable Clusters (+Interaction)
Tool Set 2
Tool Set 3
Placement and Routing Architecture
Control, Computation and Memory Units
Reconfigurable Media Processor

Fig. 34

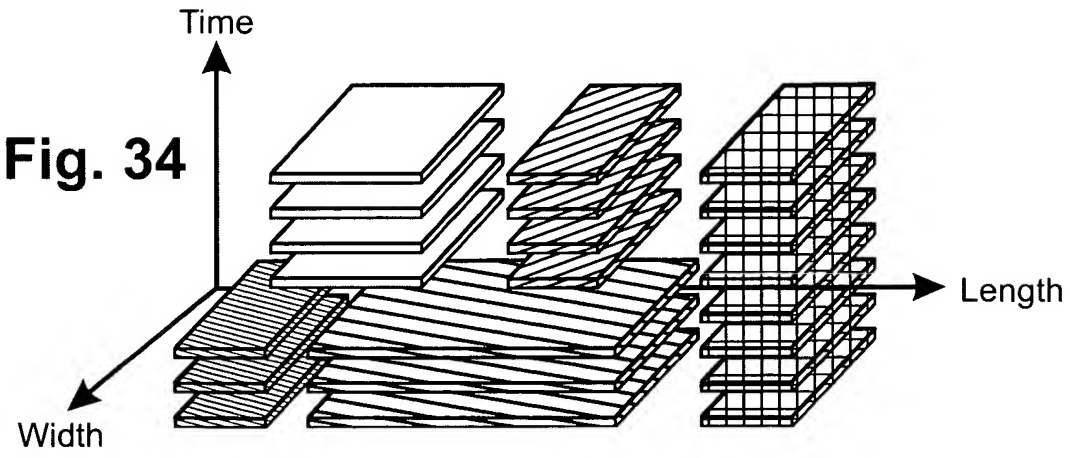

Time
Length
Width

Fig. 35

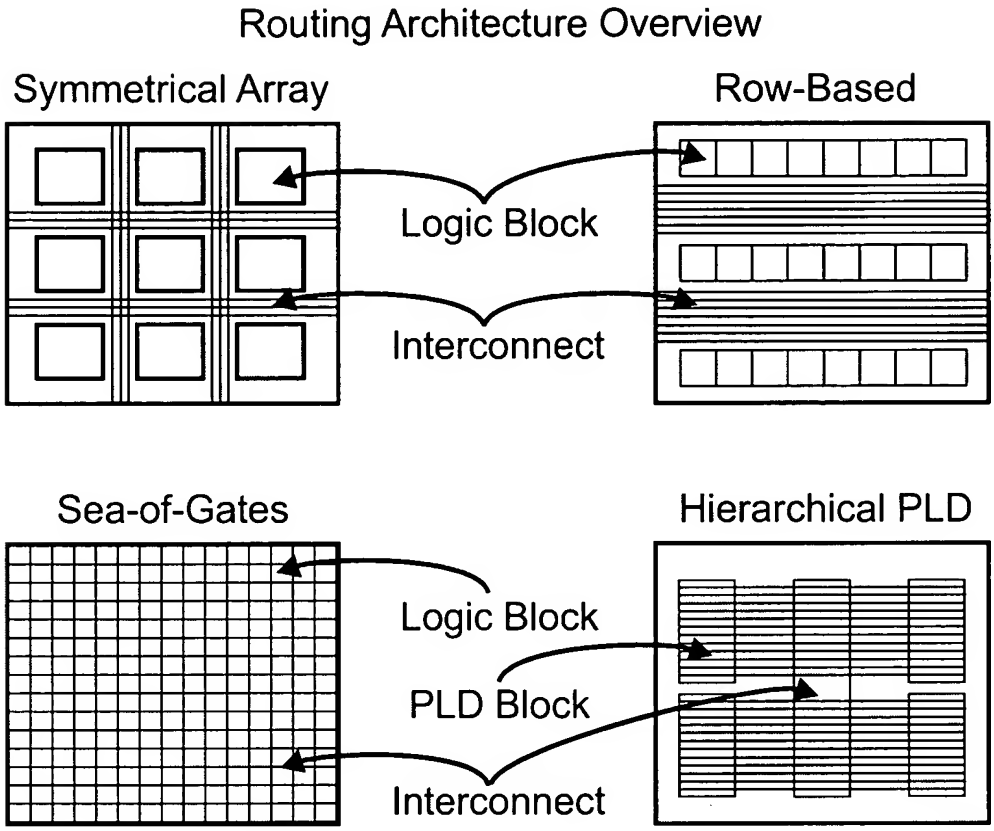

Routing Architecture Overview
Symmetrical Array
Row-Based
Logic Block
Interconnect
Sea-of-Gates
Hierarchical PLD
Logic Block
PLD Block
Interconnect

Fig. 36

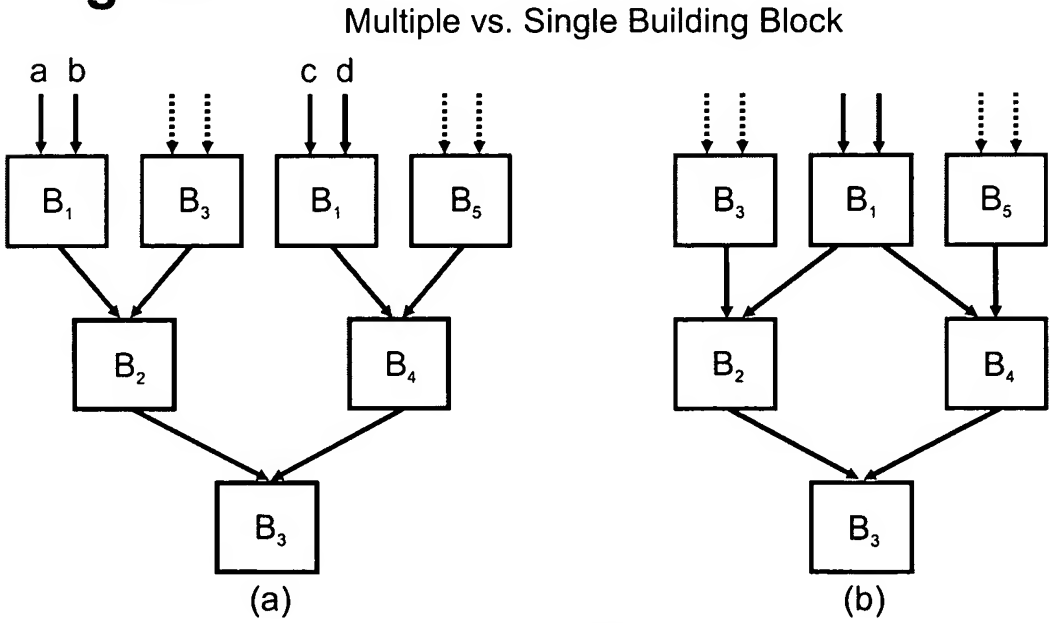

Multiple vs. Single Building Block
a b
c d
B1
B3
B1
B5
B2
B4
B3
(a)
B3
B1
B5
B2
B4
B3
(b)

Fig. 37

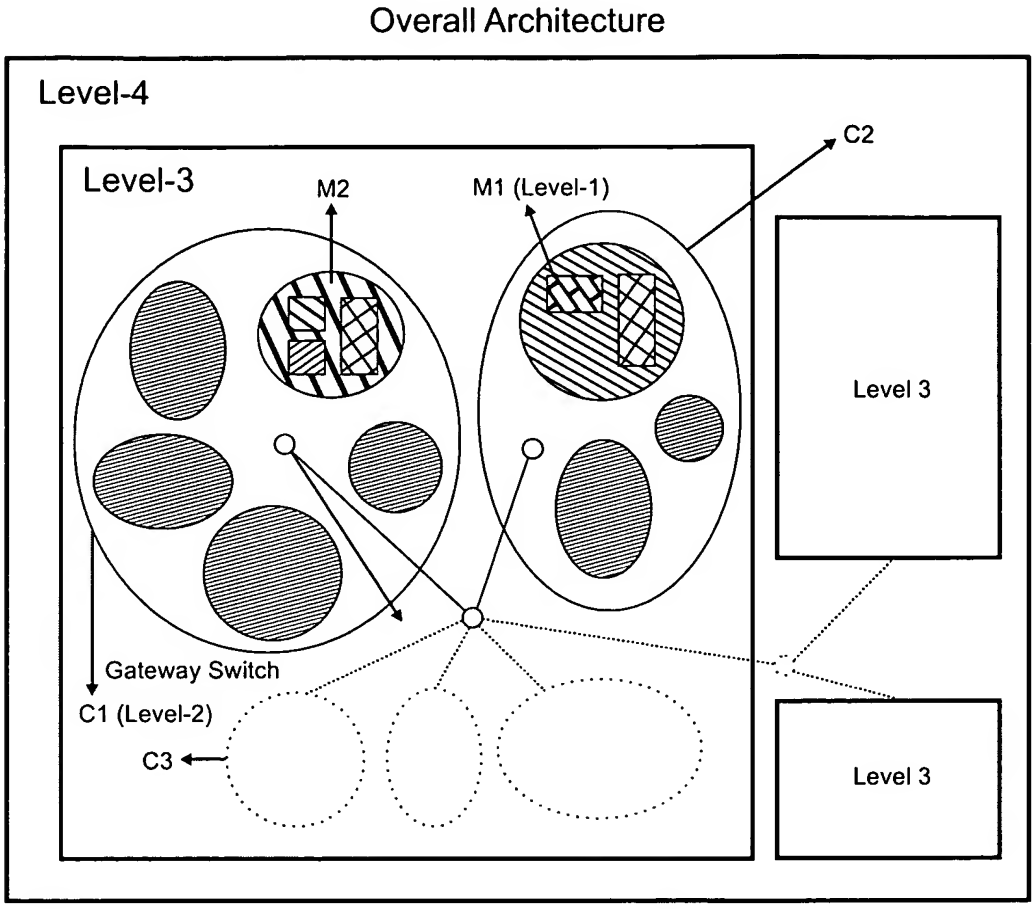

Overall Architecture
Level-4
Level-3
M2
M1 (Level-1)
C2
Level 3
Gateway Switch
C1 (Level-2)
C3
Level 3

Fig. 38

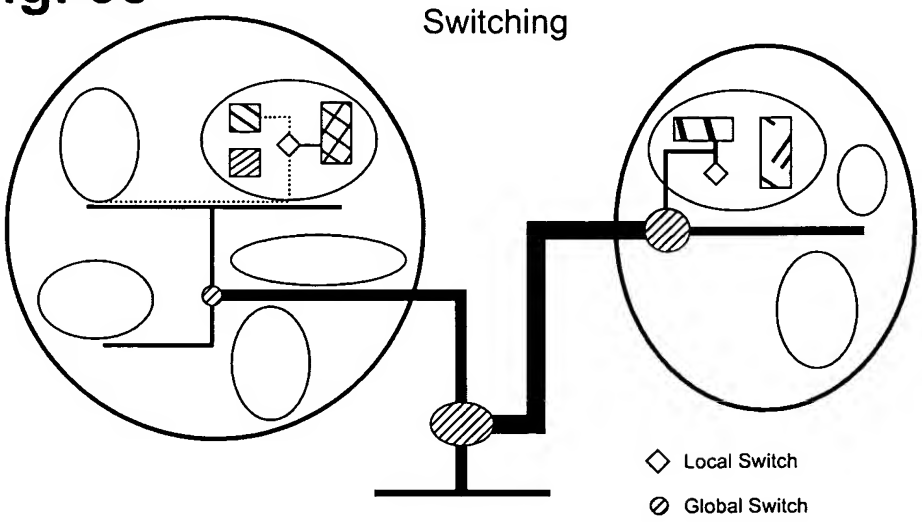

Switching
Local Switch
Global Switch

Fig. 39

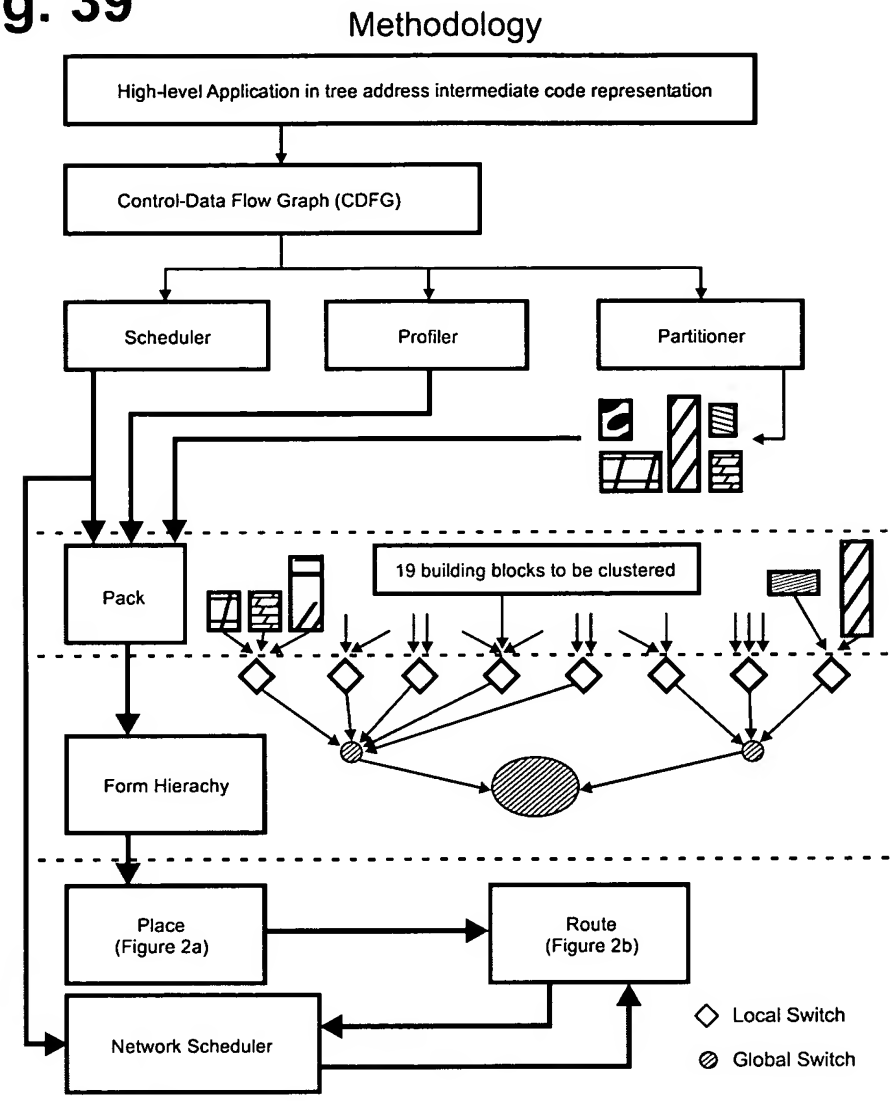


Fig. 40A

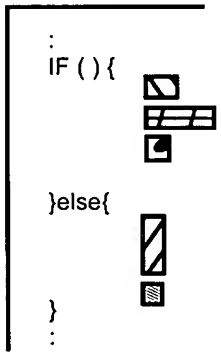


Fig. 40B

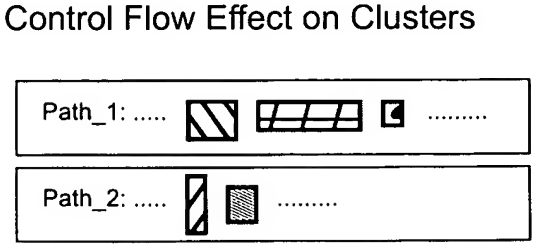


Fig. 41A

Cost Matrix

	A	B	C	D	E	F
A	0	X	X	X	X	X
B	5	0	X	X	X	X
C	6	0	0	X	X	X
D	4	3	7	0	X	X
E	1	4	1	0	0	X
F	3	0	4	5	3	0

Fig. 41B

Pre-Placement

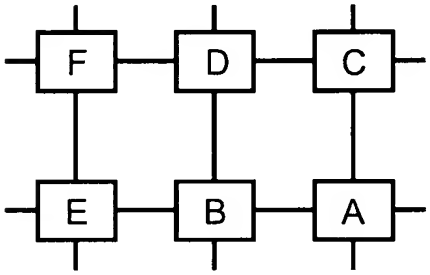


Fig. 42

Design Flow

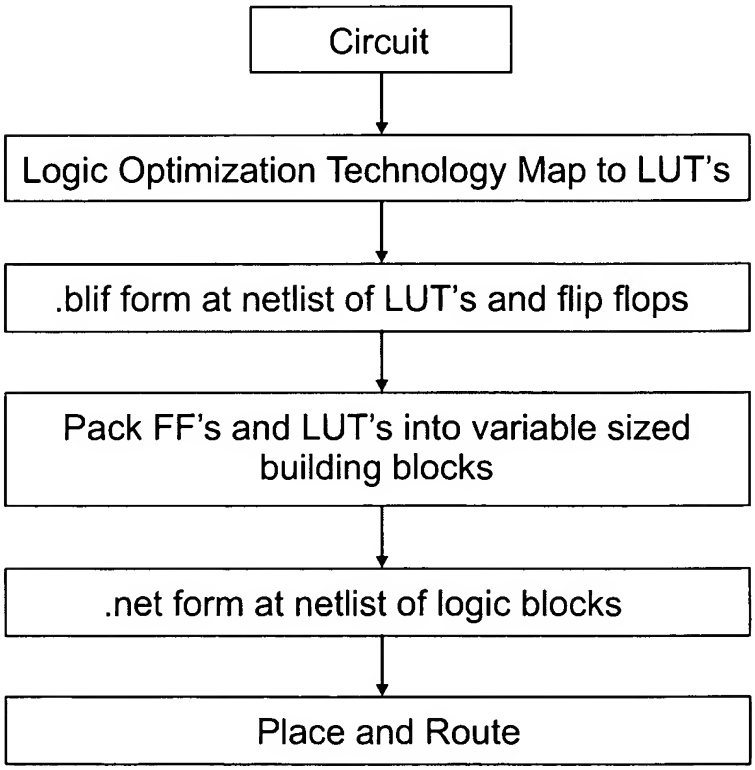


Fig. 43

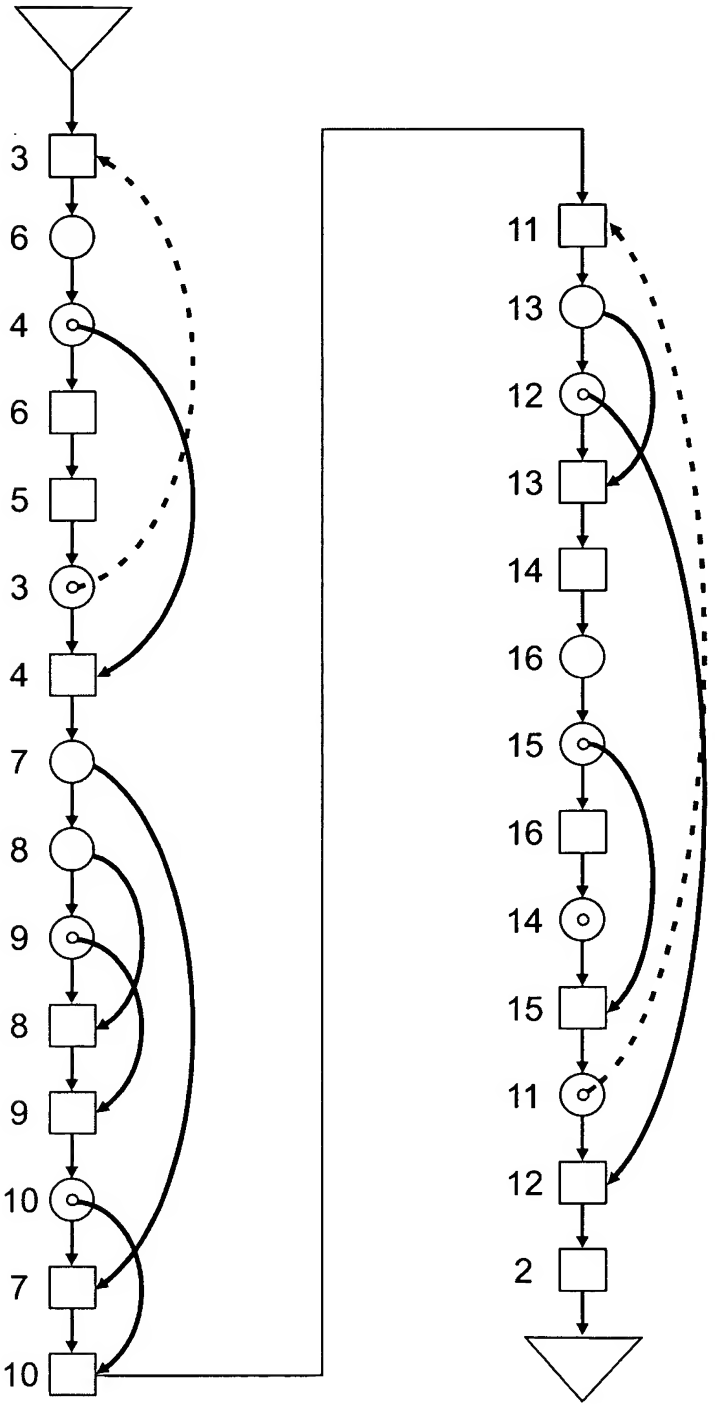

Control Flow Linked List
3
6
4
6
5
3
4
7
8
9
8
9
10
7
10
11
13
12
13
14
16
15
16
14
15
11
12
2

Fig. 44

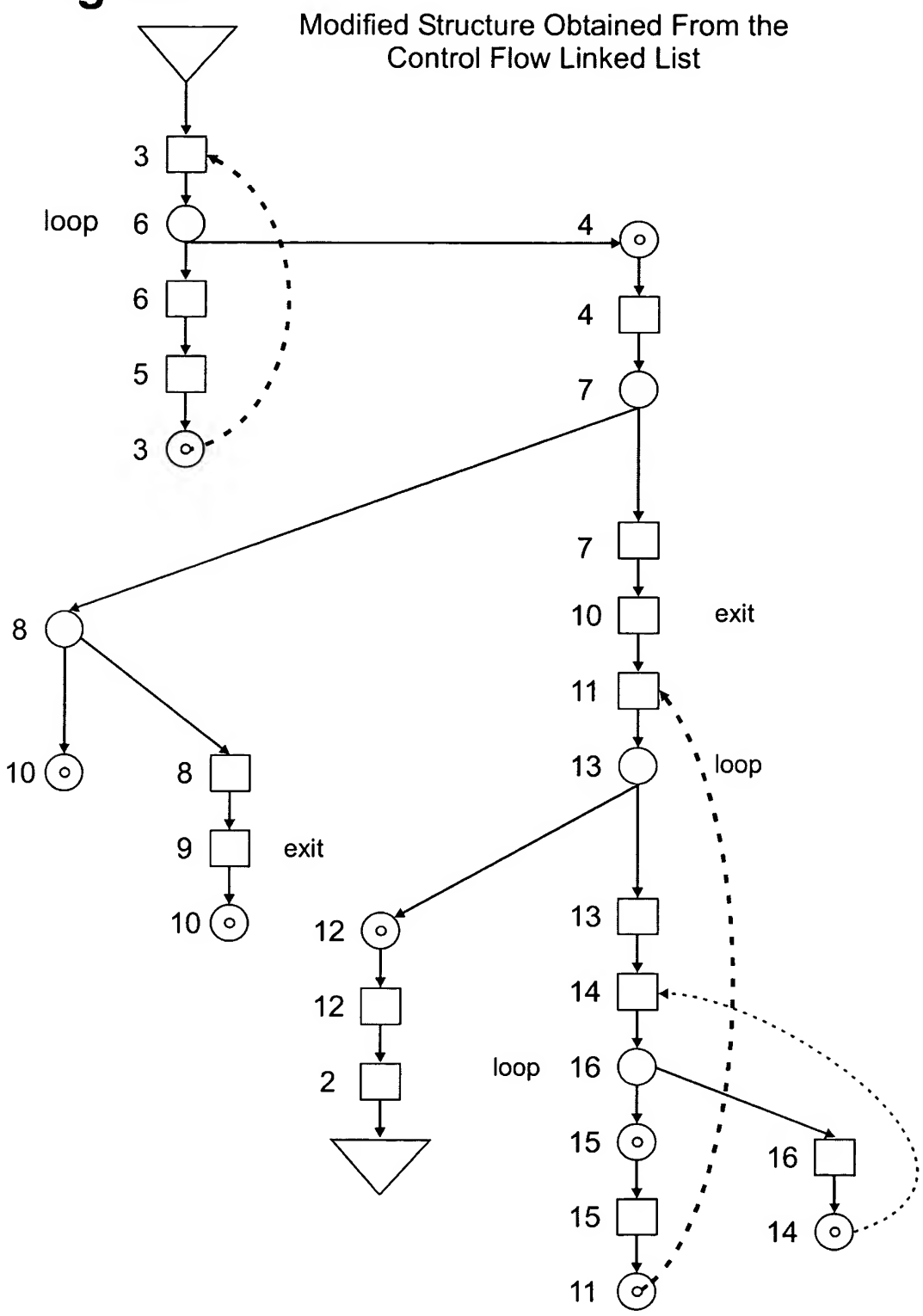

Modified Structure Obtained From the Control Flow Linked List
3
loop
6
6
5
3
4
4
7
7
10
exit
11
13
loop
8
10
8
9
exit
10
12
12
2
13
14
loop
16
15
15
11
16
14

Fig. 45

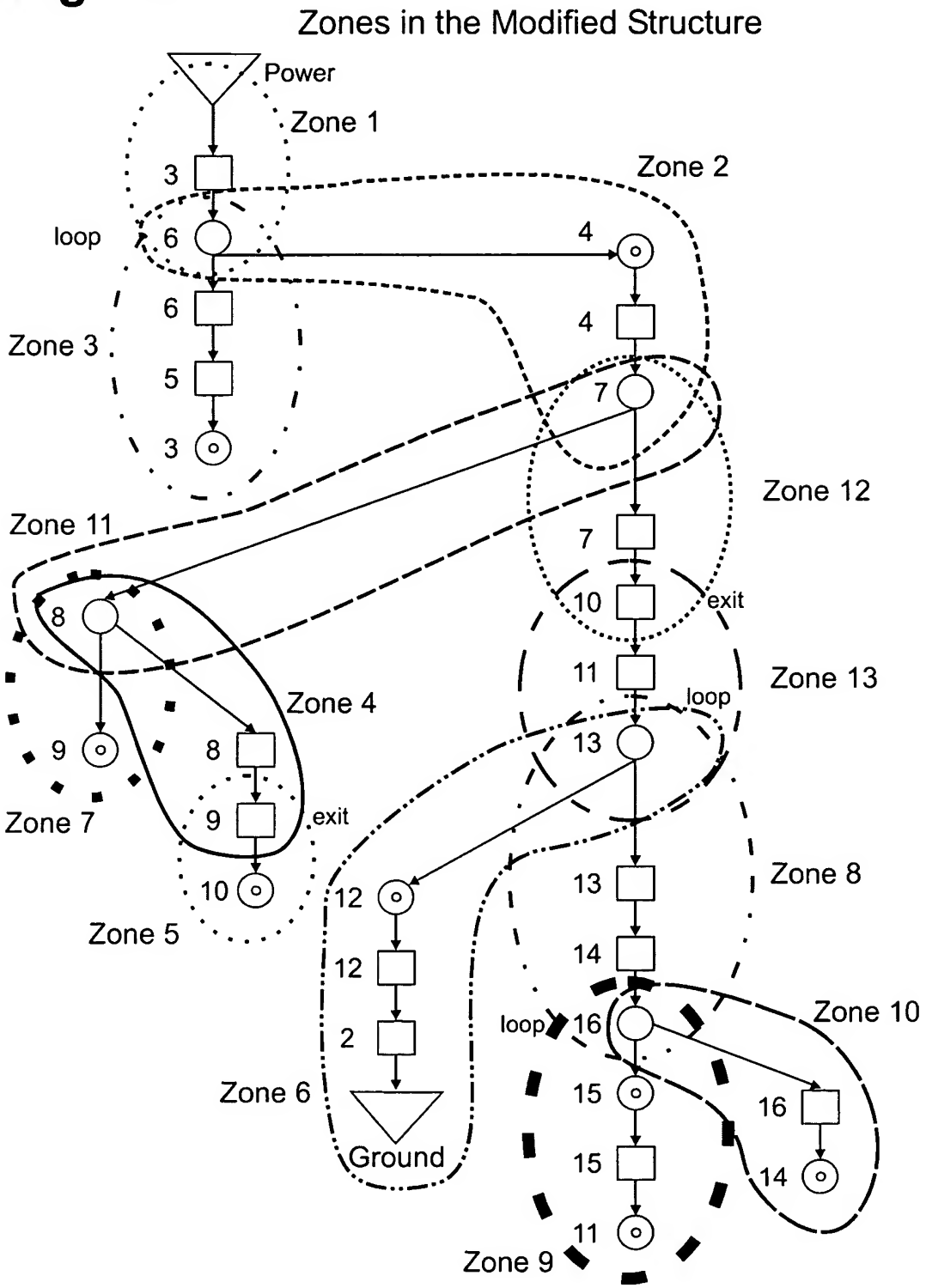
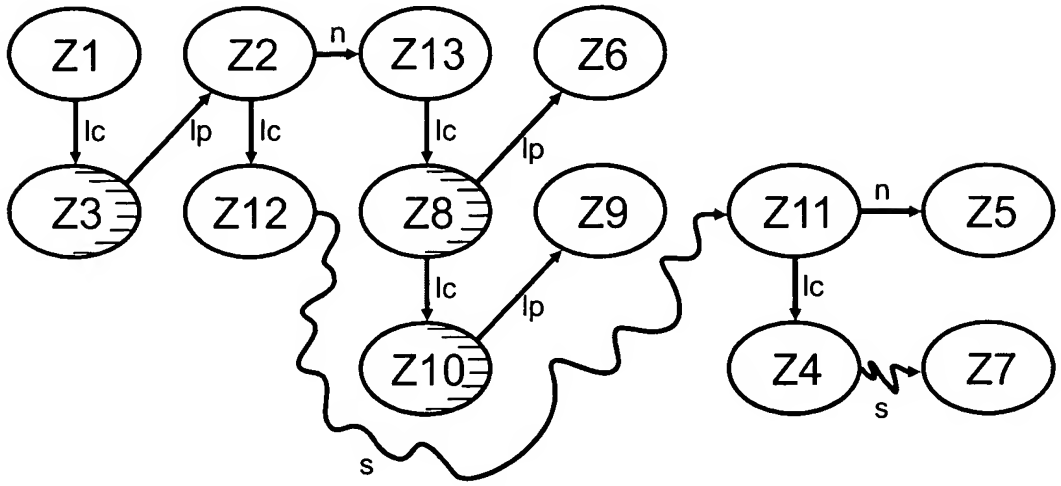

Zones in the Modified Structure
Power
Zone 1
Zone 2
Zone 3
Zone 4
Zone 5
Zone 6
Zone 7
Zone 8
Zone 9
Zone 10
Zone 11
Zone 12
Zone 13
loop
exit
Ground

Fig. 46

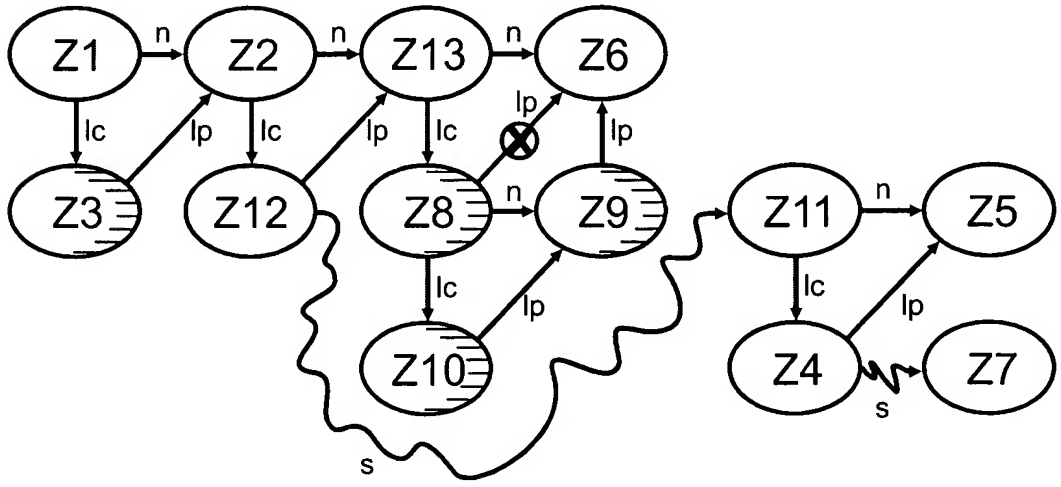
Initial Zone Structure Obtained



s: sibling relationship
lc: later child relationship
lp: later parent relationship
In all types, destination zone is (lc/s/lp) of source zone.
The shaded zones are Loop types.

Fig. 47

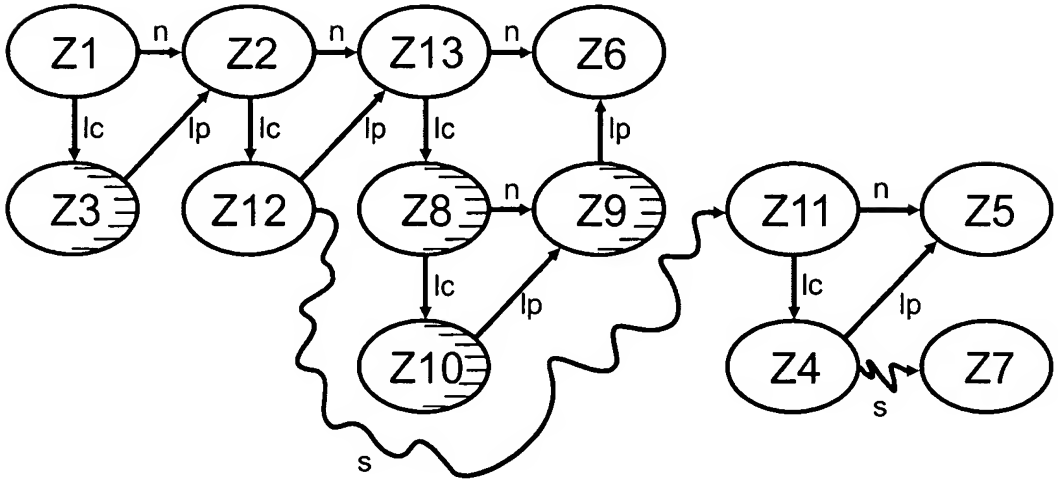
Comprehensive Zone Structure
with Cancelled Links Shown



s: sibling relationship
lc: later child relationship
lp: later parent relationship
In all types, destination zone is (lc/s/lp) of source zone.
The shaded zones are Loop types.

Fig. 48

Comprehensive Zone Structure
with Cancelled Links Removed



s: sibling relationship
lc: later child relationship
lp: later parent relationship
In all types, destination zone is (lc/s/lp) of source zone.
The shaded zones are Loop types.

Fig. 49

Sequentially Ordered Zones